

GM21 LCD TV

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Approval	Organization	Signature	Date
		CHY	04-05-17

Pinout diagram of the CN1 connector. The diagram shows a vertical connector with pins numbered 1 to 26. Pins 1-16 are labeled on the left, and pins 17-26 are labeled on the right. A blue oval encloses pins 1-16, which are labeled 'Shell' at the top and bottom. A red arrow points to pin 26, labeled 'GND'. A red arrow points to pin 1, labeled 'CN1'. A red arrow points to pin 26, labeled 'DVI-I'.

Pin Number	Signal Name	Signal Type
1	Shell	Ground
2	RX2-	Signal
3	RX2+	Signal
4	GND	Ground
5	RX4-	Signal
6	RX4+	Signal
7	SCL	Signal
8	SDA	Signal
9	VS	Signal
10	RX1-	Signal
11	RX1+	Signal
12	GND	Ground
13	RX3-	Signal
14	RX3+	Signal
15	5V	Signal
16	GND	Ground
17	HP	Signal
18	RX0-	Signal
19	RX0+	Signal
20	GND	Ground
21	RX5-	Signal
22	RX5+	Signal
23	RD+	Signal
24	RD-	Signal
25	RED	Signal
26	GND	Ground

**DVI For
DVI Port**

EDID DVI

DIGITAL

Pinout diagram for the 24AA02 I2C EEPROM:

Pin	Signal
1	A0
2	A1
3	A2
4	GND
5	SDA
6	SCL
7	WP
8	VCC

Chip Label: 24AA02
ANALOG DDC

Pr/R R22 47R 1% C3 0.01uF SOG_MC55 5

Y/G R25 47R 1% C6 0.01uF RED+ 5

Pb/B R28 47R 1% C7 0.01uF RED- 5

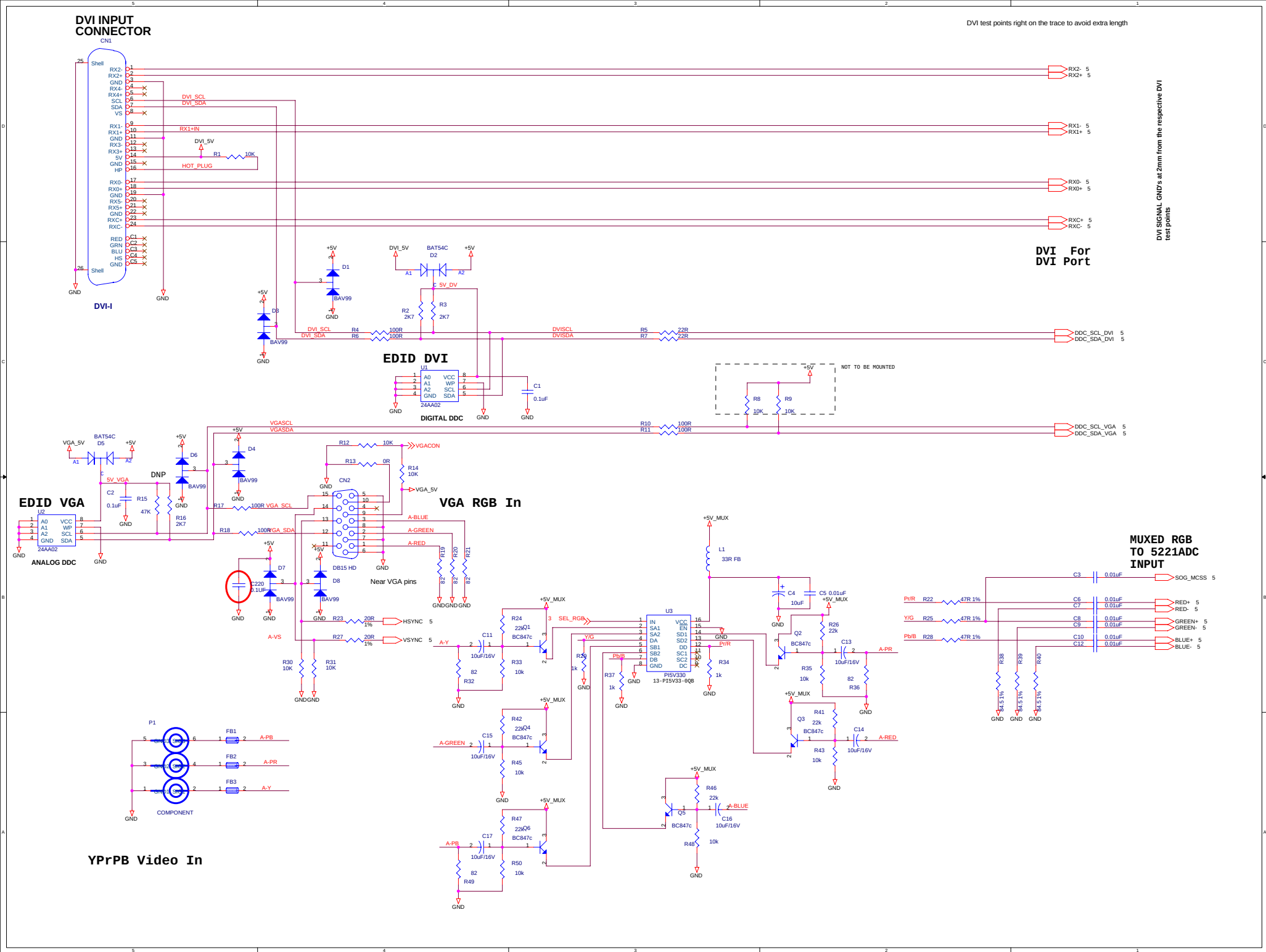
C8 0.01uF GREEN+ 5

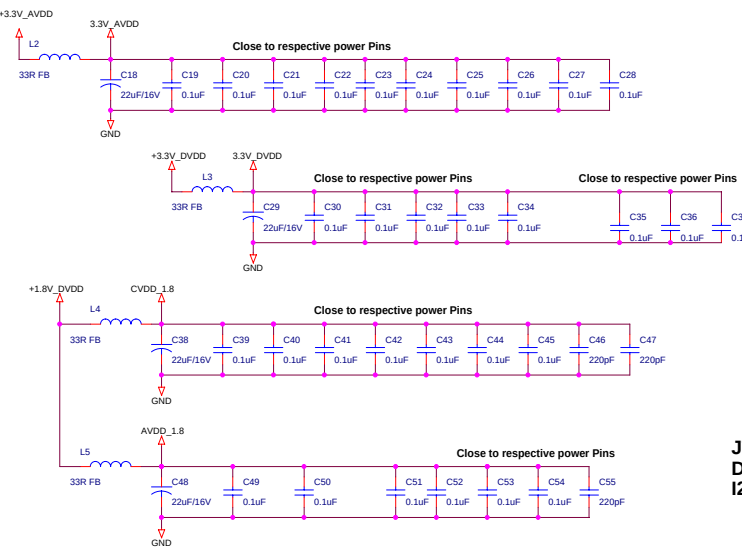
C9 0.01uF GREEN- 5

C10 0.01uF BLUE+ 5

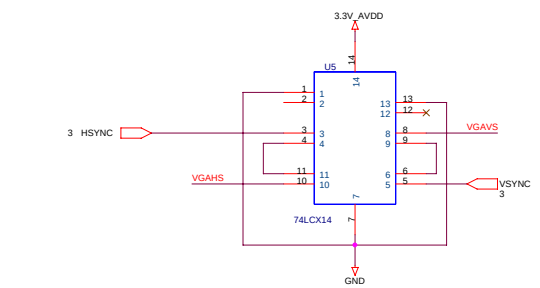
C12 0.01uF BLUE- 5

The diagram illustrates a three-phase test setup. A source labeled 'P1' is connected to three parallel lines. Each line contains a switch (SW1, SW2, SW3) and a fault breaker (FB1, FB2, FB3). The fault breakers are connected to a common busbar labeled 'COMPONENT'. The fault breakers are labeled A-PB, A-PR, and A-Y respectively.

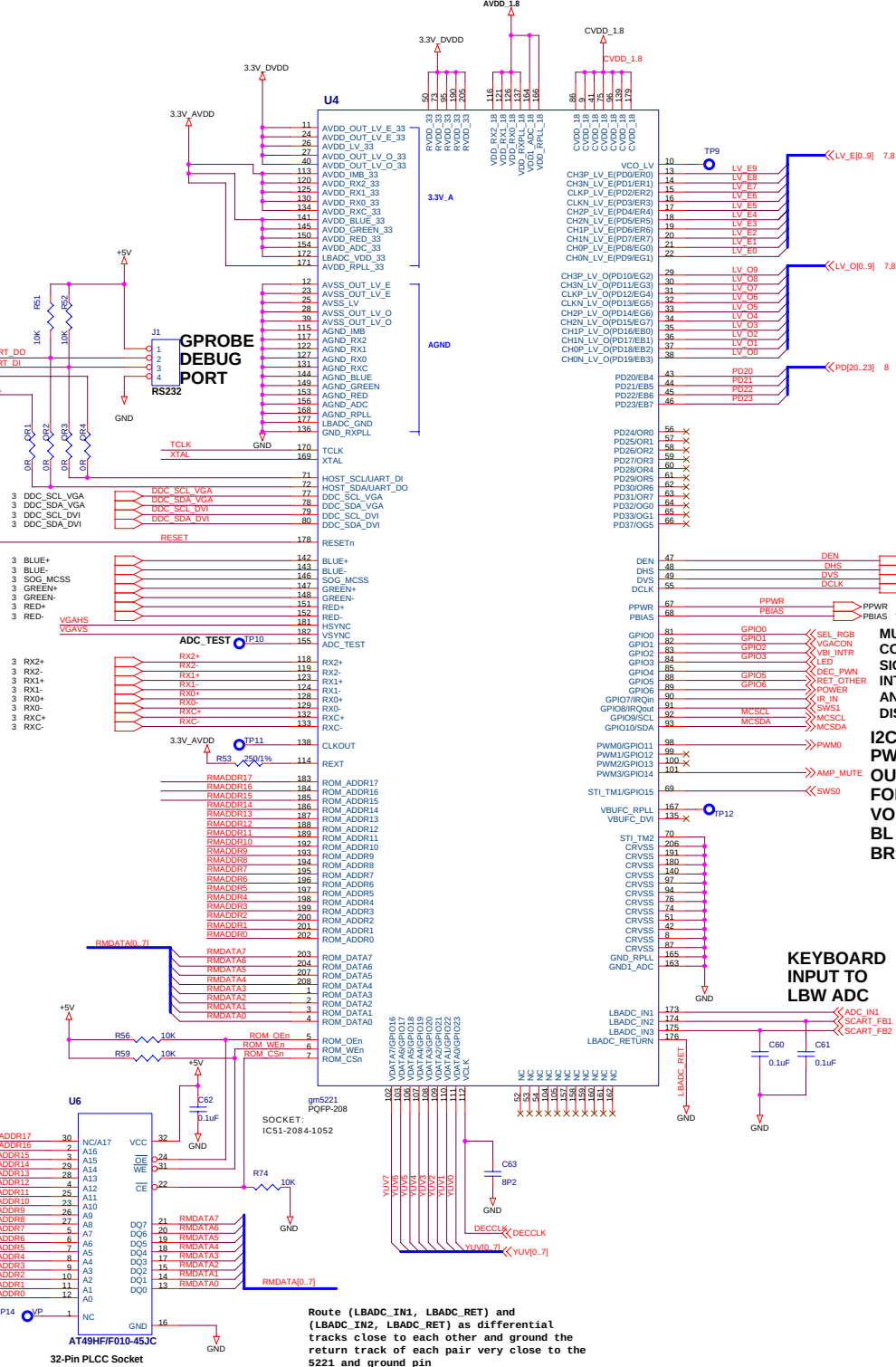
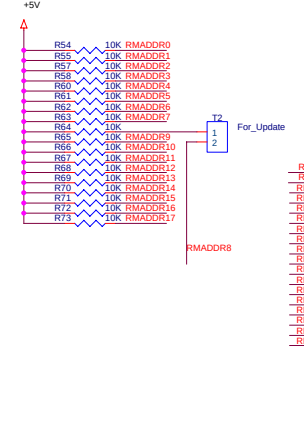




Rootstrap Signals	
RMADDR[6:0]	For I2C address [6:0] to JTAG bridge Host VF, to determine device address.
RMADDR[12:7]	User_Bits[5:0] for configuration setting
RMADDR[14:13]	OP_MODE[1:0]: 00 = Normal op. UART in 186 on system pins. 01 = I2C to JTAG bridge. 10 = JTAG port, 5 wires. 11 = External parallel control bus using ROM Addr/Data
RMADDR15	SPI_LEN: 0 = parallel ROM IF. 1 = SPI serial ROM and Cache control
RMADDR16	Initial state of OCM ROM: 0 = internal ROM on, and mapped to top 32K of OCM and OCM boot will be from internal ROM code. 1 = internal ROM off. The external ROM mapped to entire upper 512K of OCM address. OCM boot from external ROM code.
RMADDR17	OSC_SEL: 0 = Xtal and internal oscillator. 1 = TTL oscillator (on TCLK pin)



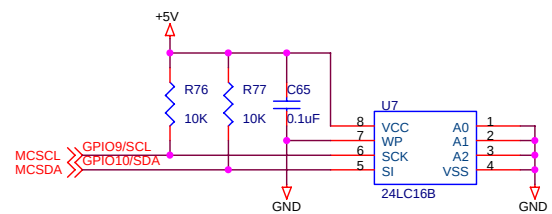
BOOTSTRAP OPTIONS SELECT (NOT POPULATED SHOULD BE HARD WIRED)



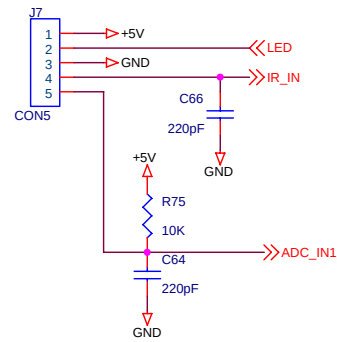
Route (LBADC_IN1, LBADC_RET) and (LBADC_IN2, LBADC_RET) as differential tracks close to each other and ground the return track of each pair very close to the 5221 and ground pin

Keypad
INTERFACE

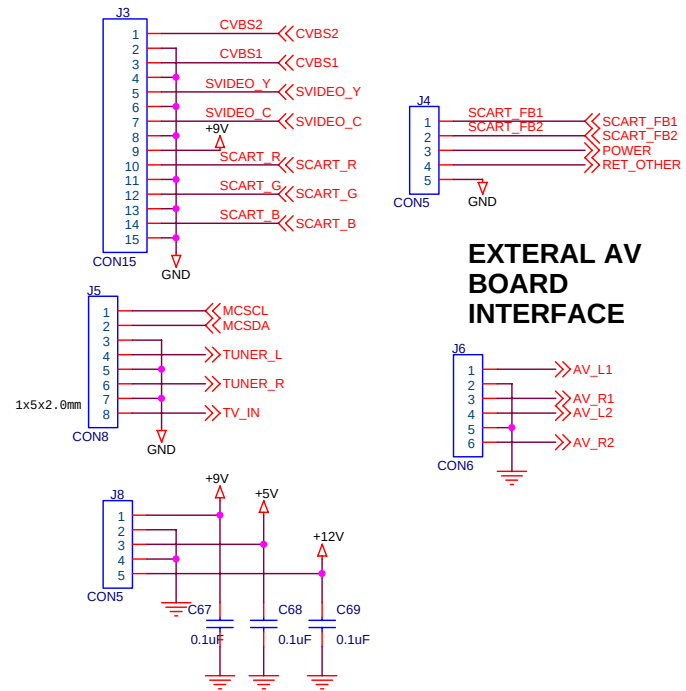
NV RAM
INTERFACE

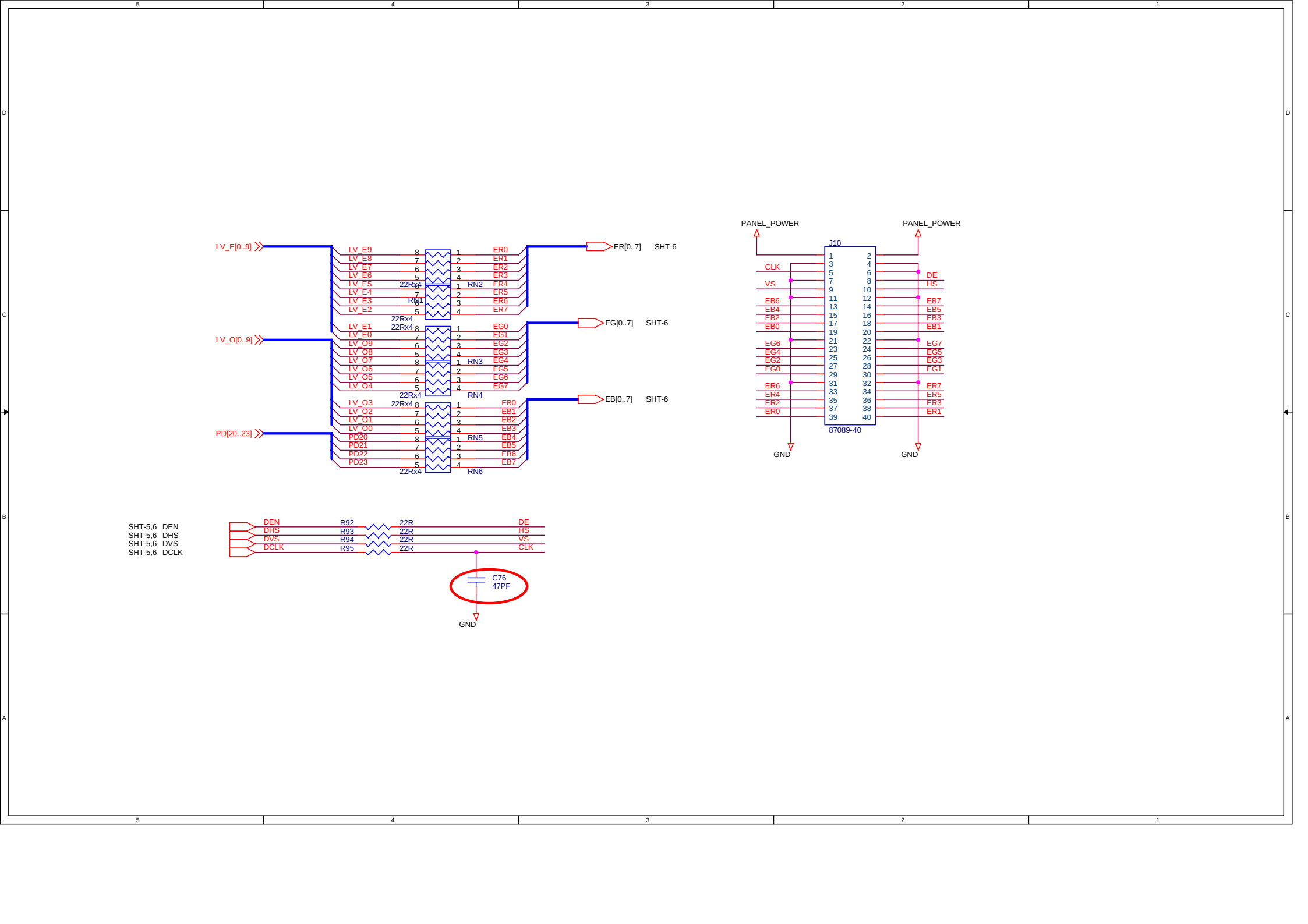


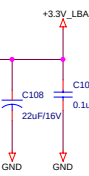
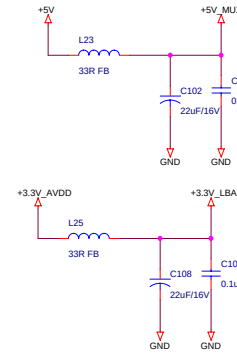
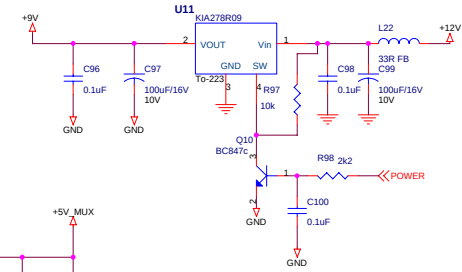
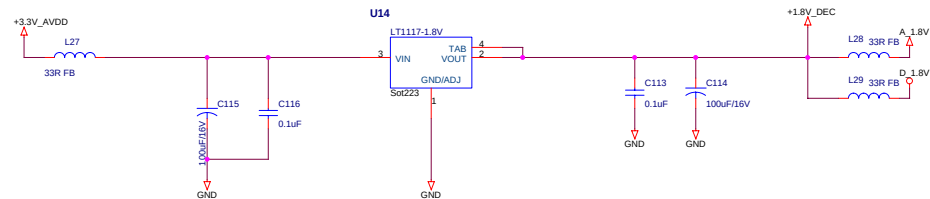
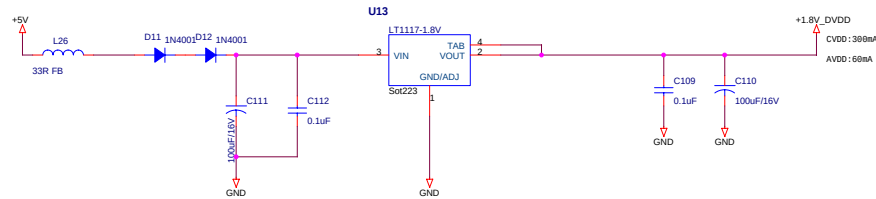
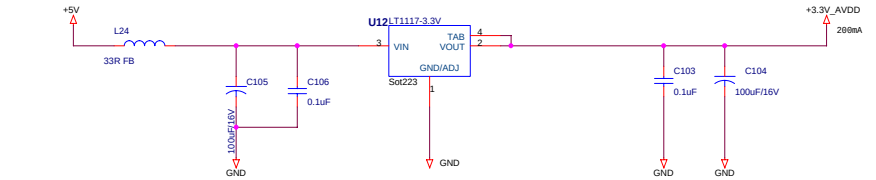
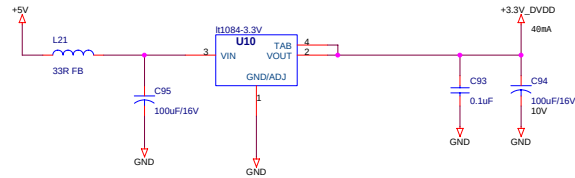
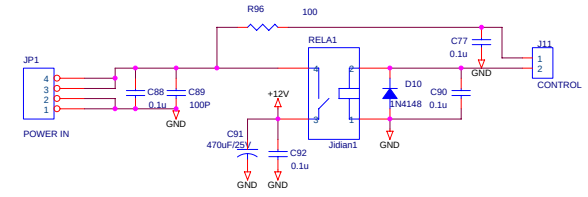
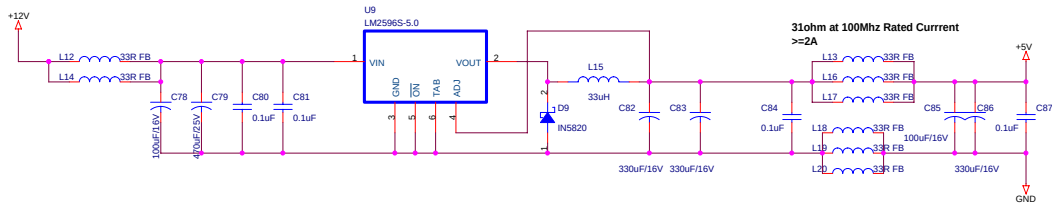
IR REMOTE SENSOR
INTERFACE

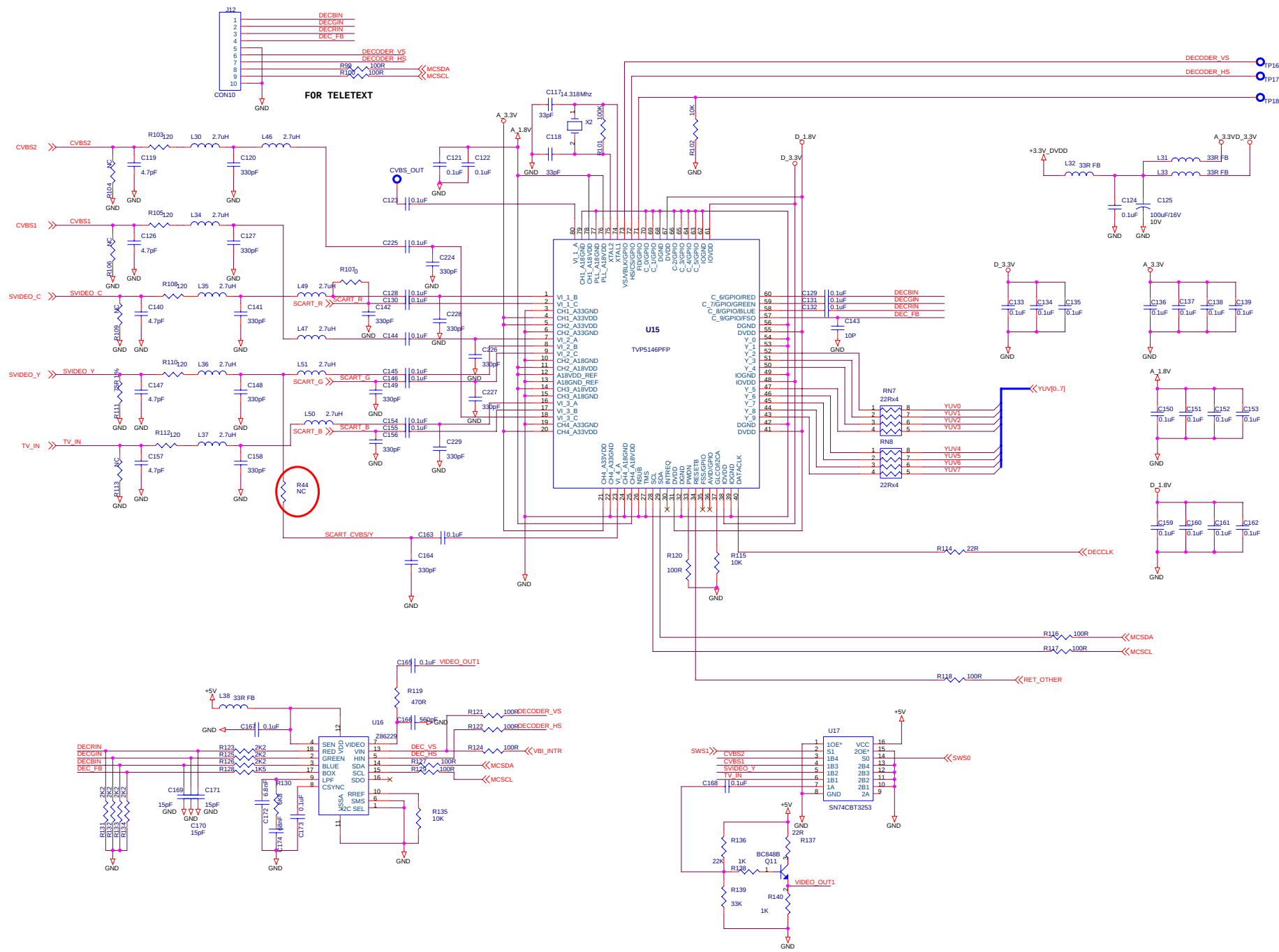


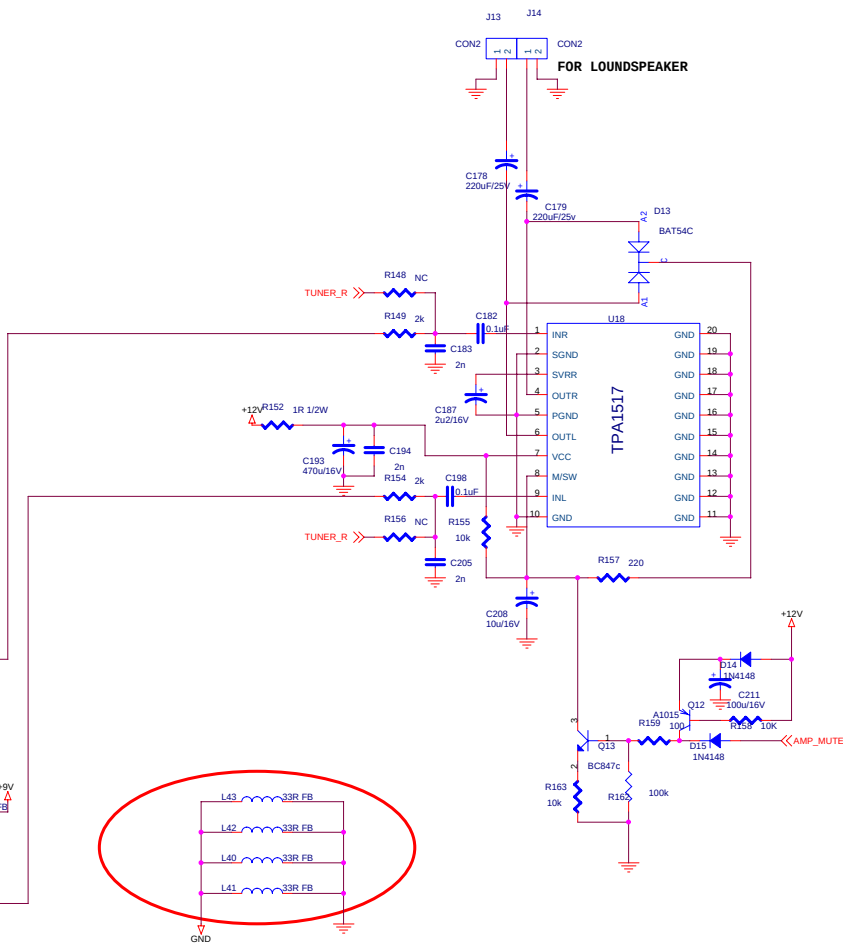
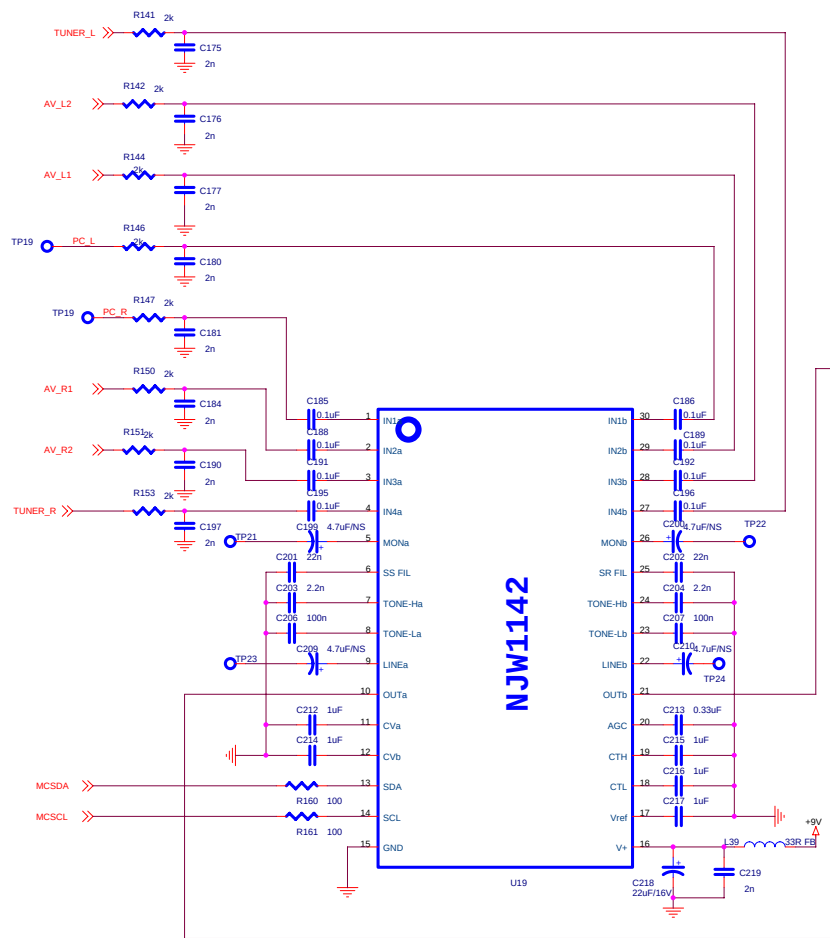
EXTERAL AV
BOARD
INTERFACE



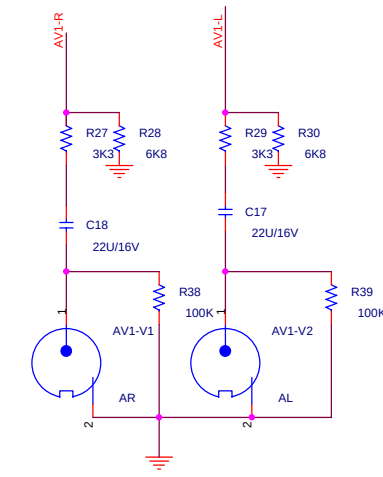
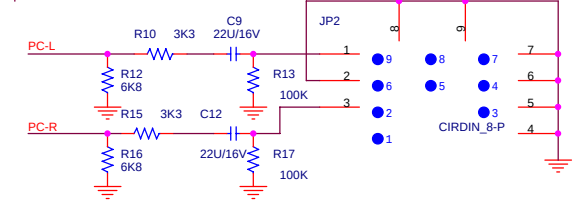
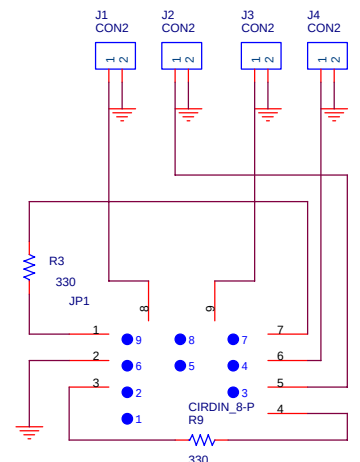
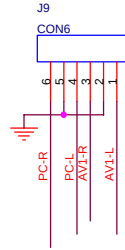
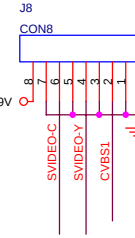
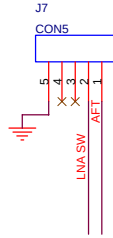
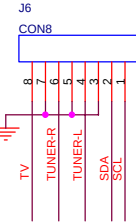
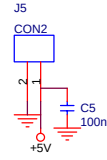
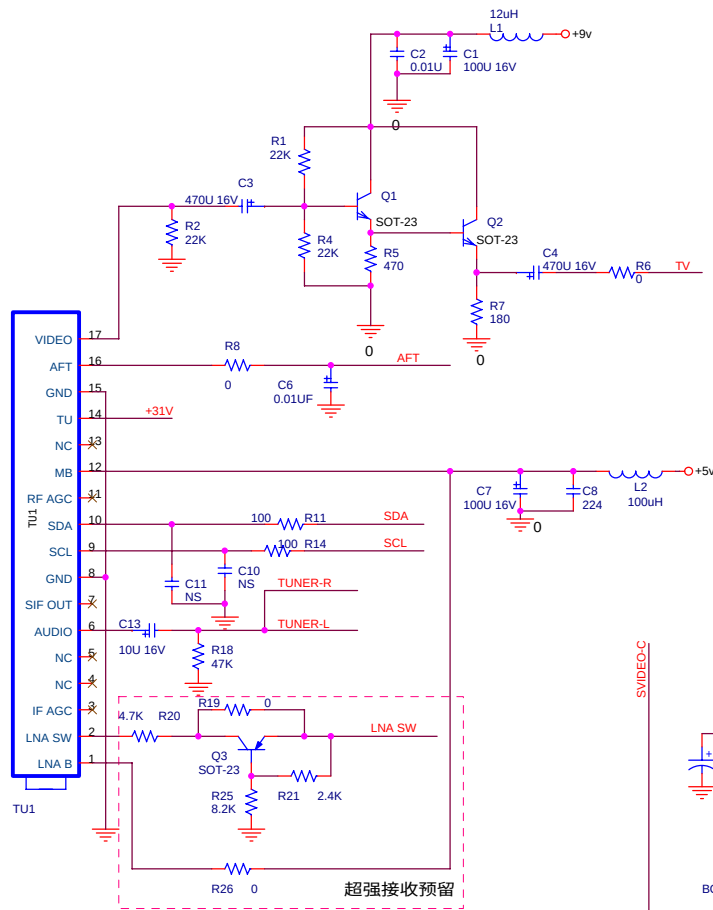








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