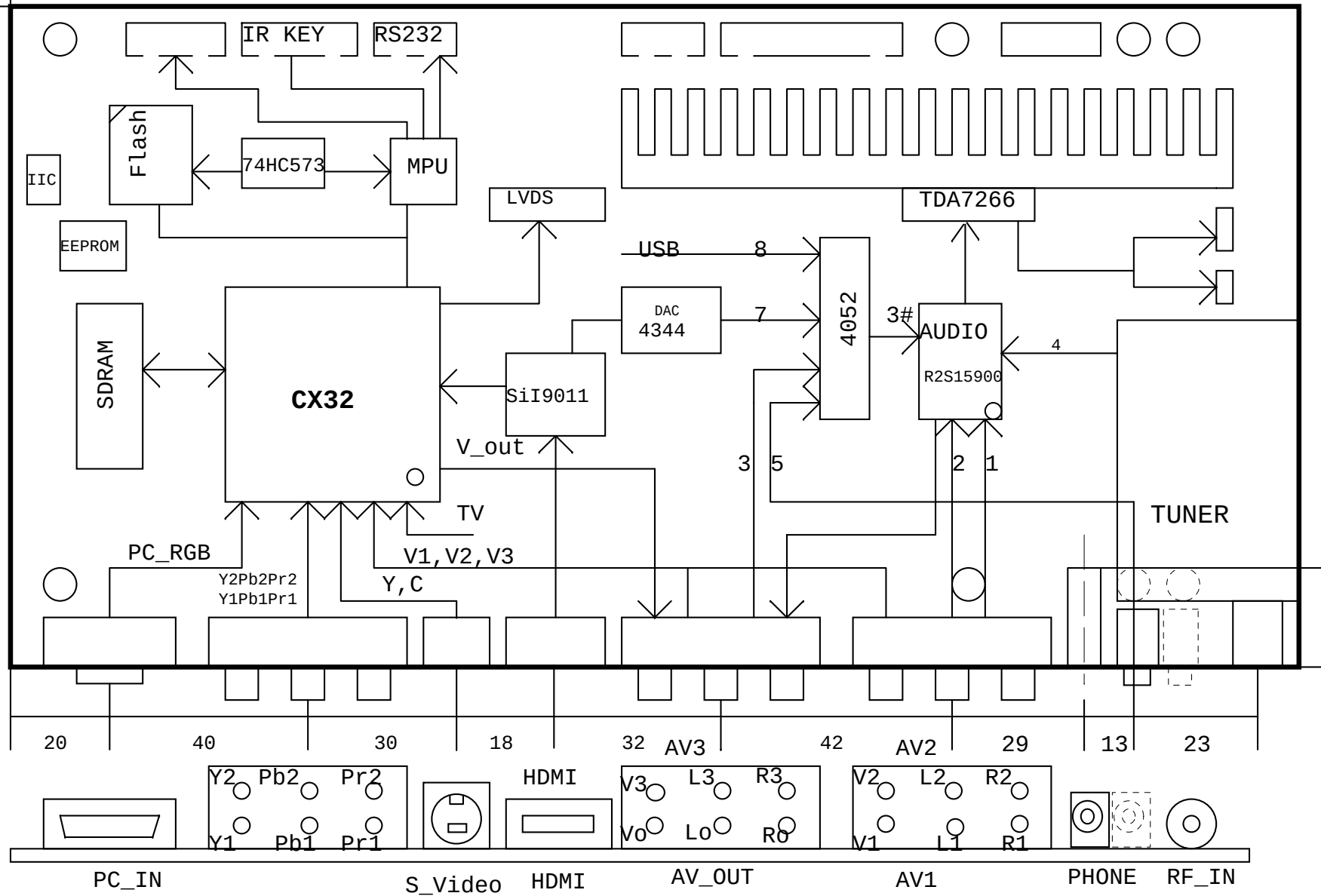


155

260

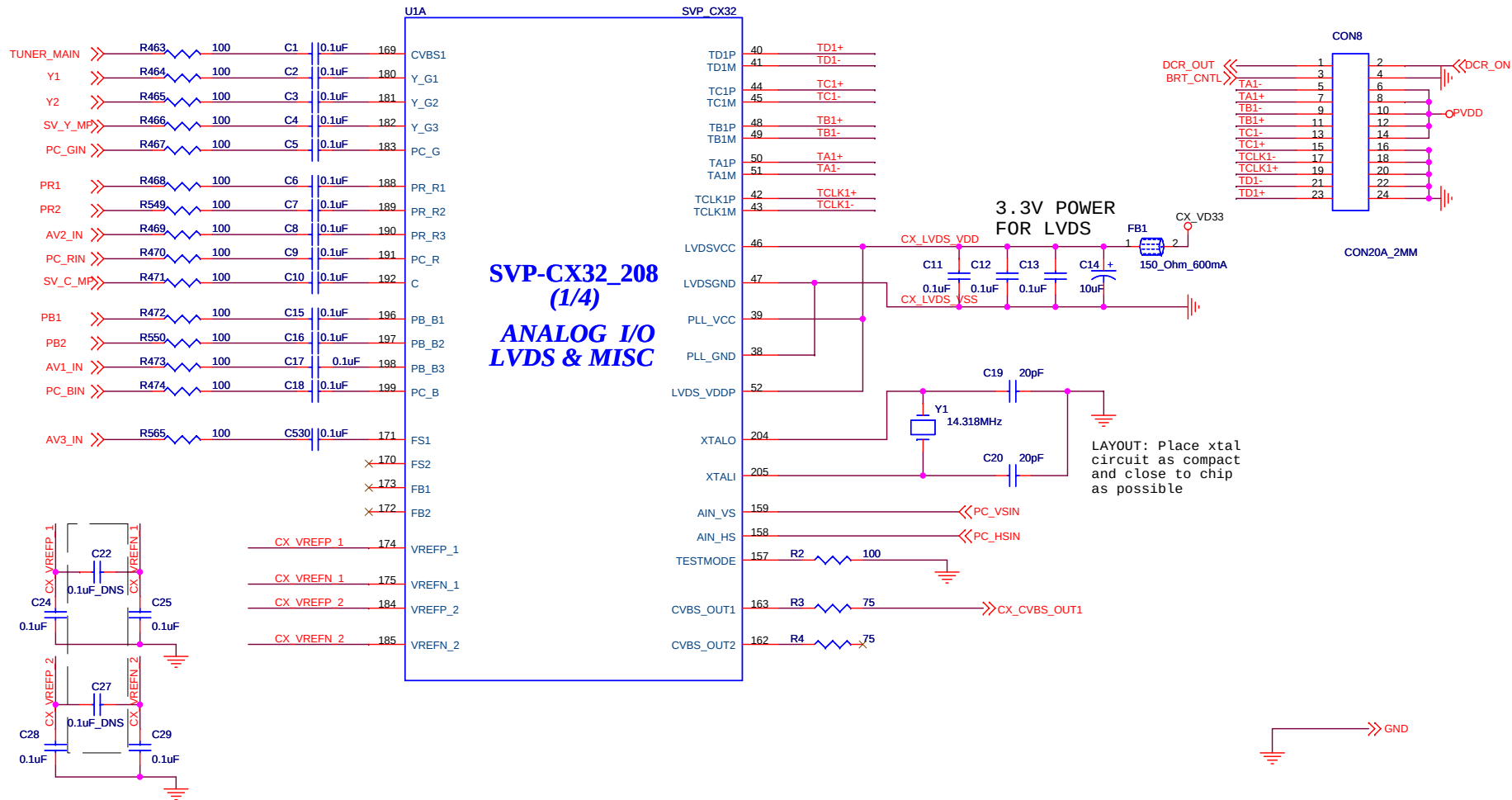


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Title		
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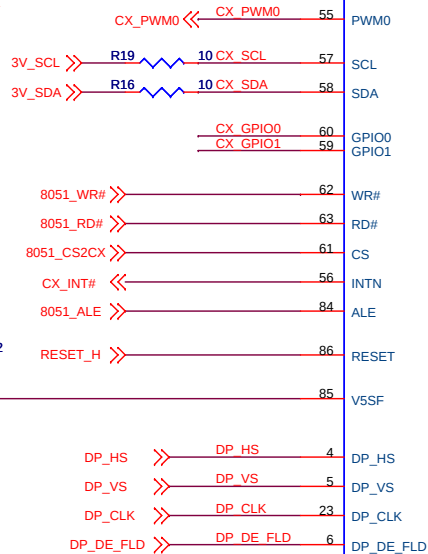
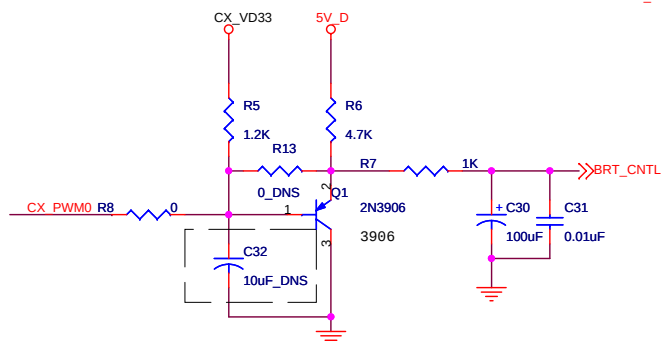
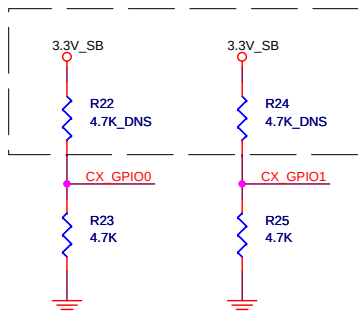


Pin Name	DEFINITION IN LCD251
CVBS1	MAIN TUNER INPUT
Y_G3	S_Video Y in
PB_B3	AV1 CVBS INPUT
PR_R3	AV2 CVBS INPUT
FS1	AV3 CVBS INPUT

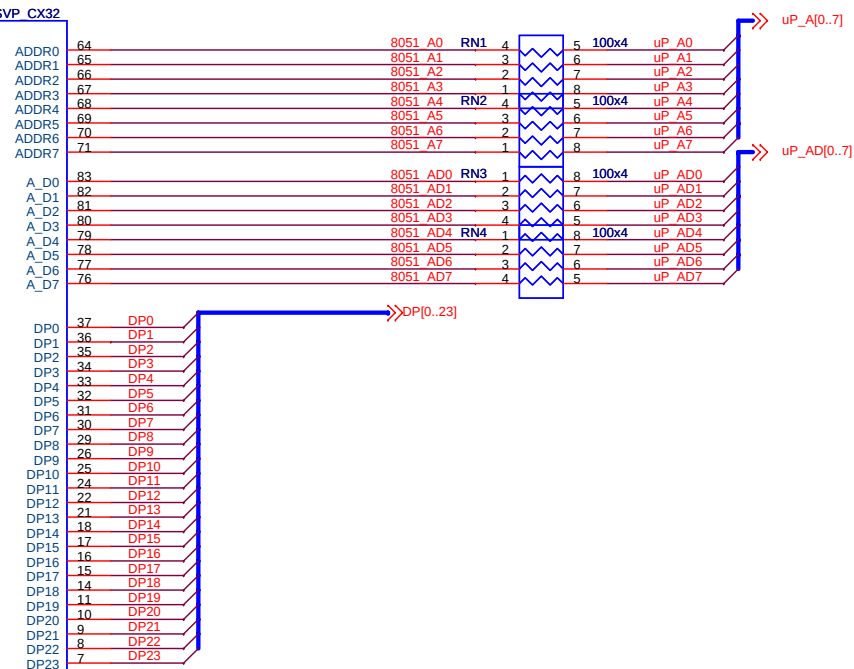
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SVP-CX32_208 (2/4) CPU INTERFACE DIGITAL OUT



Pin Name	Pin No.	1 (HIGH)	0 (LOW)
GPIO0		MPU in A/D Multiplex Mode	MPU in A/D Separate Mode
GPIO1		Use Rising Edge of WR# to latch data	Use Falling Edge of WR# to latch data

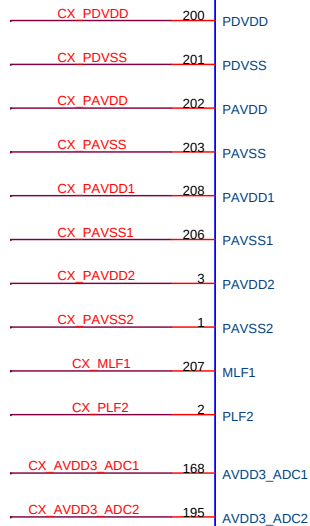
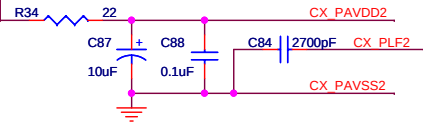
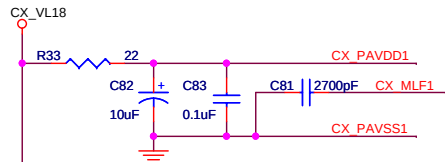
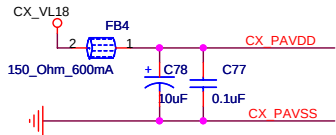
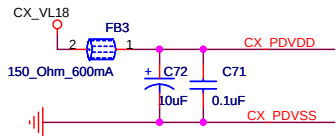
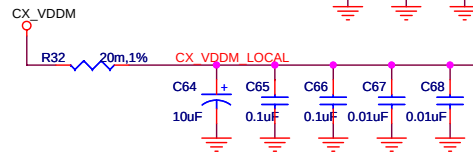
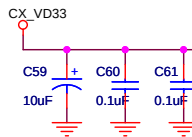
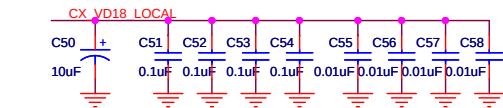
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PRELIMINARY

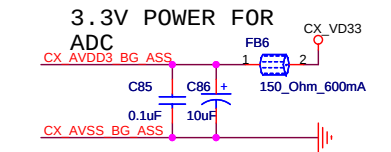
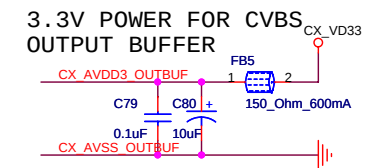
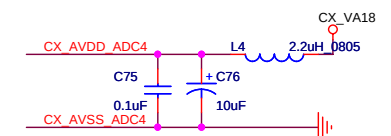
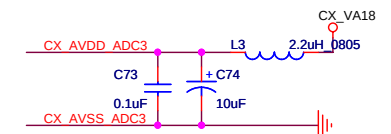
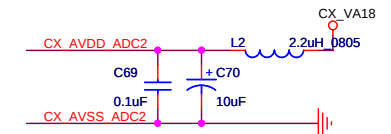
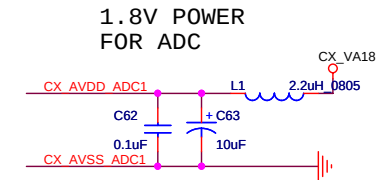
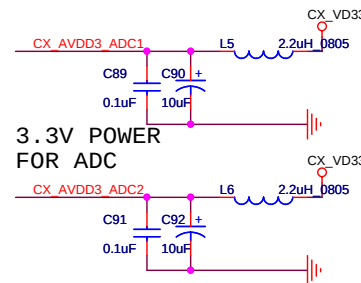
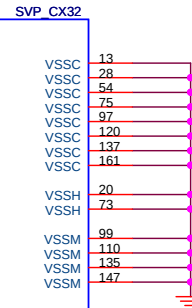


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SVP-CX32_208 (4/4) Power / Ground

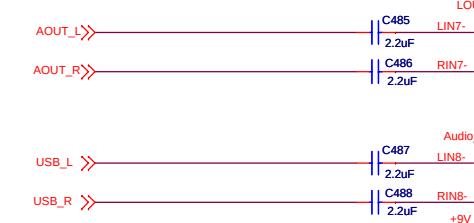
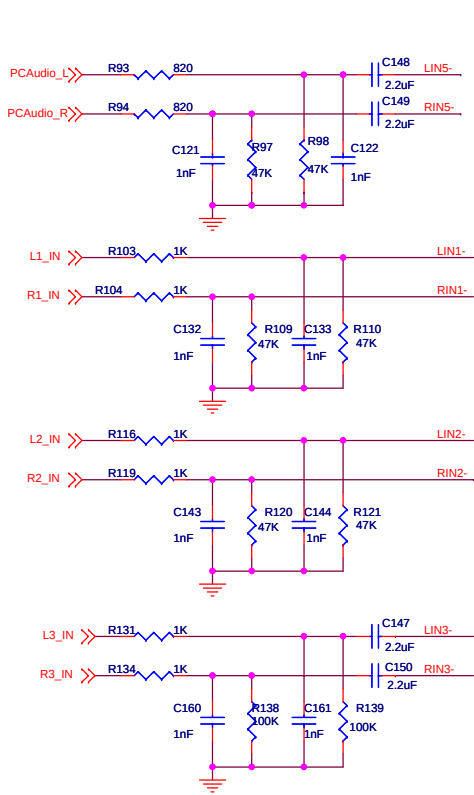


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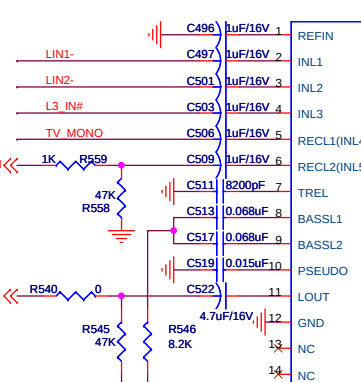
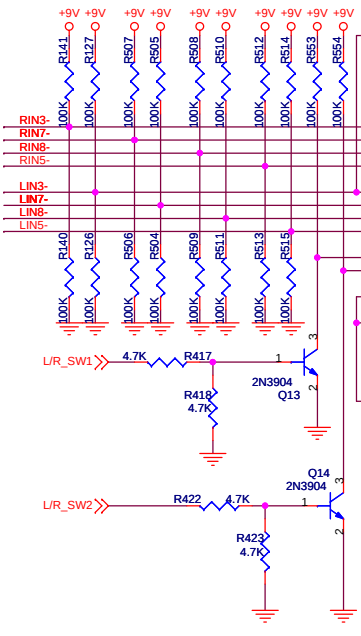


1

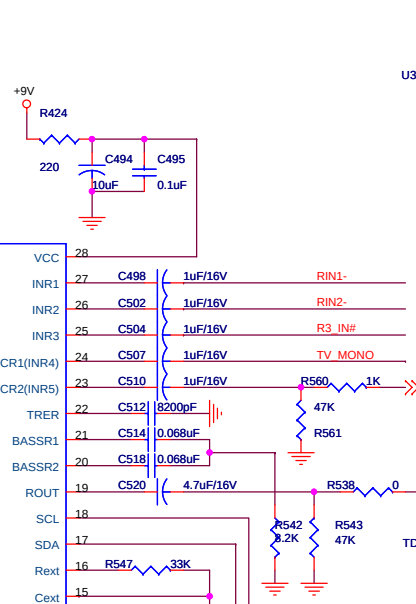
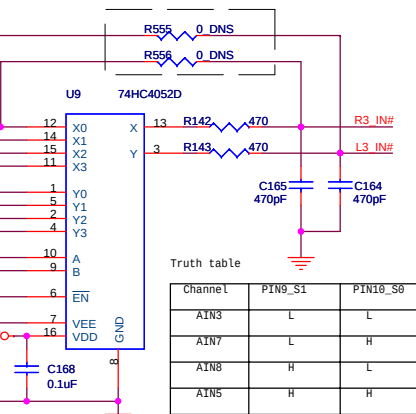
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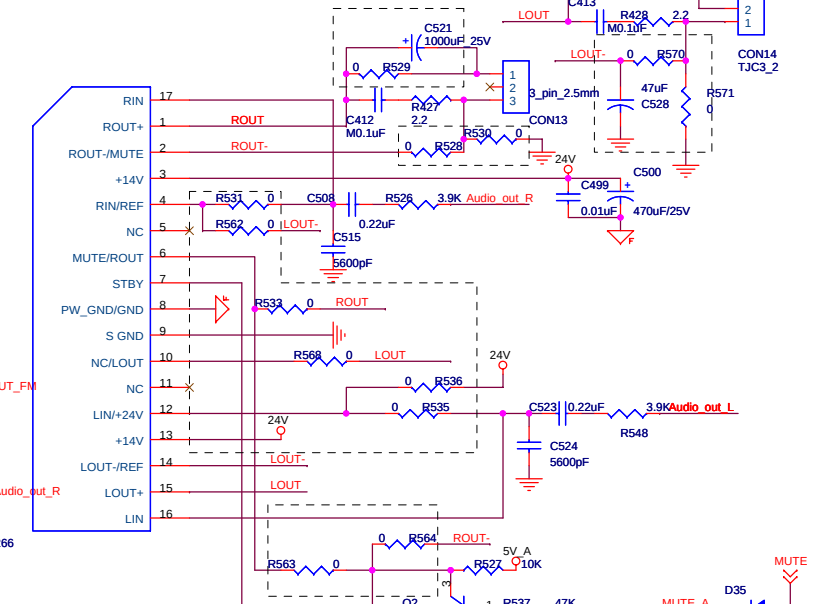
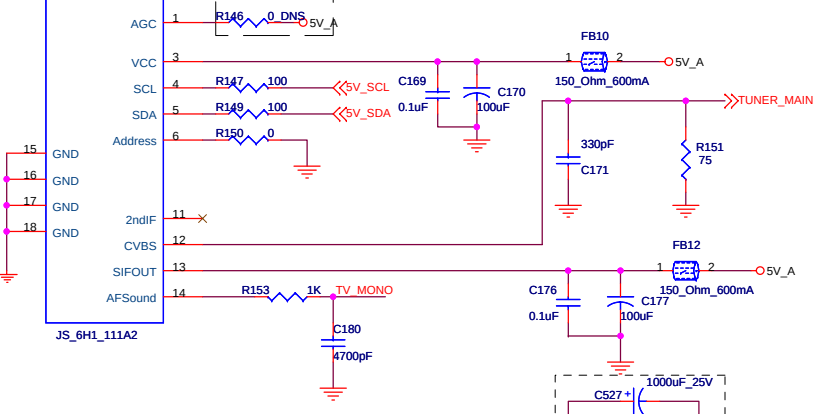
INPUT		OUTPUT
L_SW	R_SW	X,Y
0	0	0
0	1	1
1	0	2
1	1	3



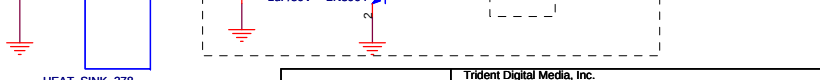
INPUT		OUTPUT
L_SW	R_SW	X,Y
0	0	0
0	1	1
1	0	2
1	1	3



INPUT		OUTPUT
L_SW	R_SW	X,Y
0	0	0
0	1	1
1	0	2
1	1	3



INPUT		OUTPUT
L_SW	R_SW	X,Y
0	0	0
0	1	1
1	0	2
1	1	3



Channel	PIN9_S1	PIN10_S8
AIN3	L	L
AIN7	L	H
AIN8	H	L
AIN5	H	H

Channel	PIN9_S1	PIN10_S8
AIN3	L	L
AIN7	L	H
AIN8	H	L
AIN5	H	H

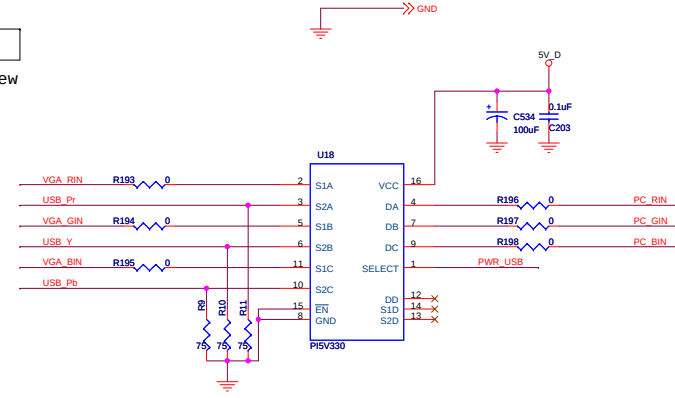
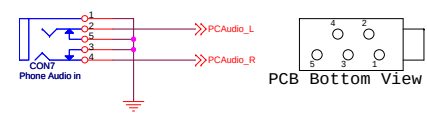
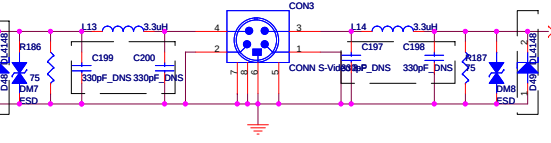
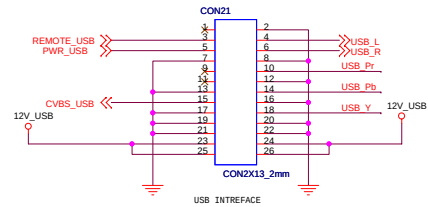
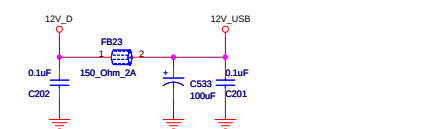
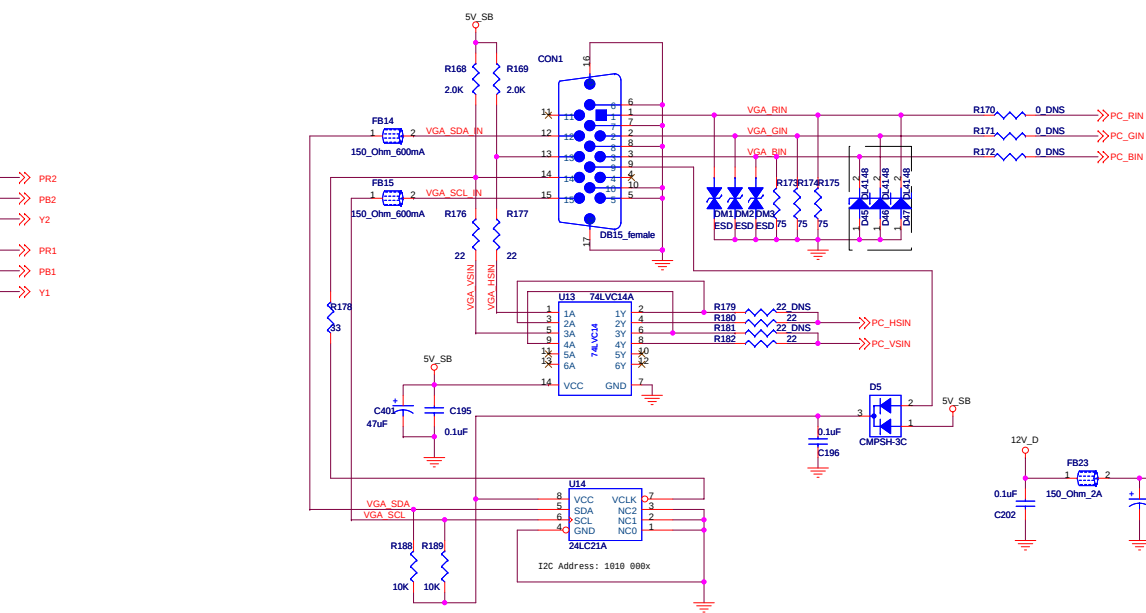
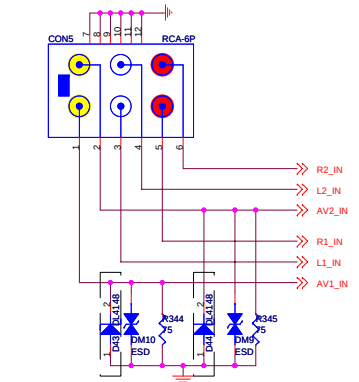
Channel	PIN9_S1	PIN10_S8
AIN3	L	L
AIN7	L	H
AIN8	H	L
AIN5	H	H

Channel	PIN9_S1	PIN10_S8
AIN3	L	L
AIN7	L	H
AIN8	H	L
AIN5	H	H

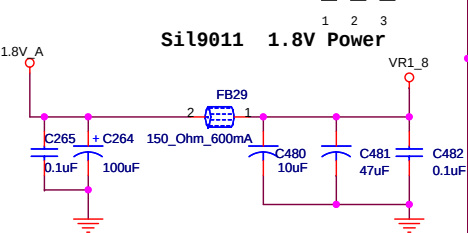
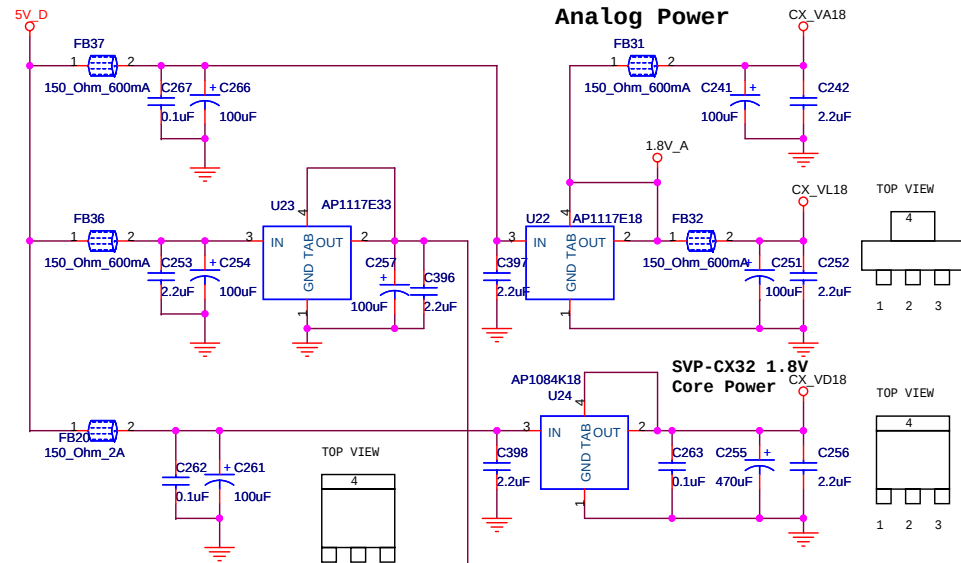
Channel	PIN9_S1	PIN10_S8
AIN3	L	L
AIN7	L	H
AIN8	H	L
AIN5	H	H

Channel	PIN9_S1	PIN10_S8
AIN3	L	L
AIN7	L	H
AIN8	H	L
AIN5	H	H

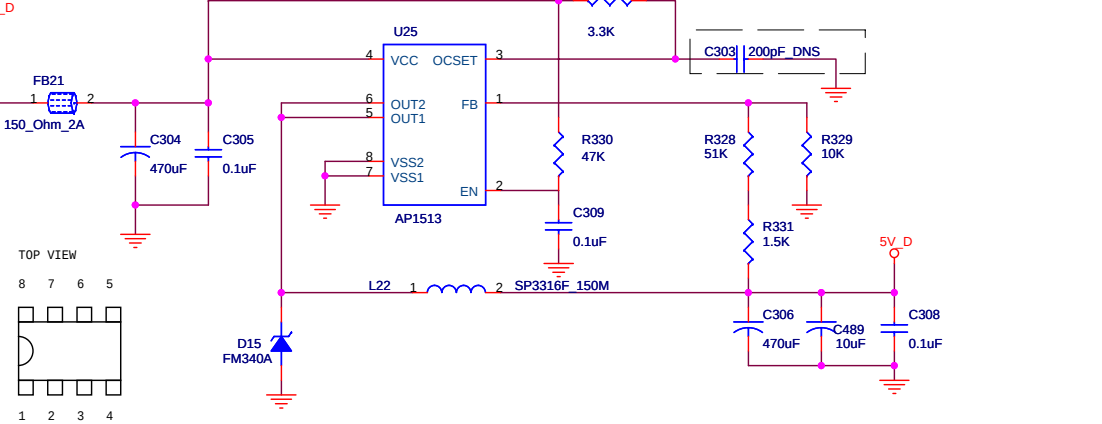
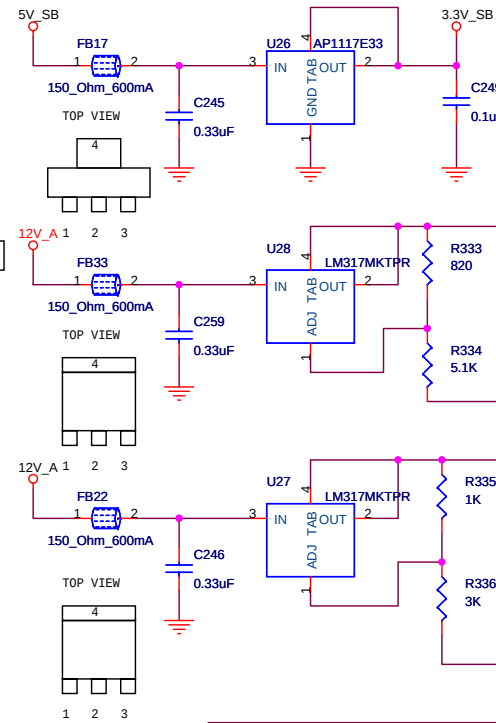
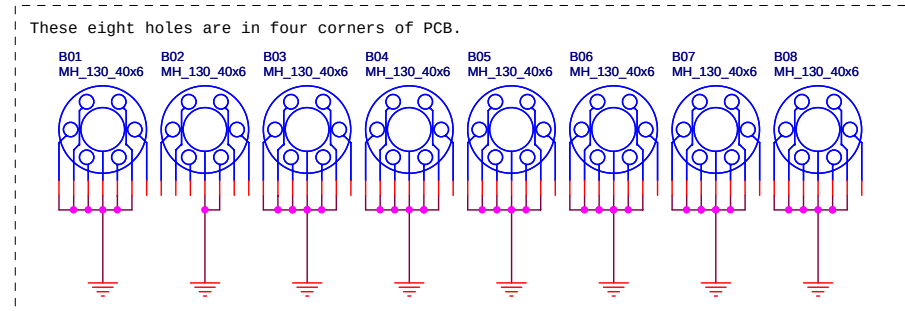
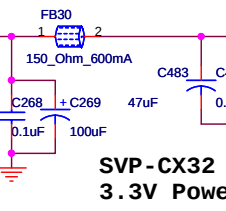
Channel	PIN9_S1	PIN10_S8
AIN3	L	L
AIN7	L	H
AIN8	H	L
AIN5	H	H



SVP-CX32 1.8V Analog Power



Sil9011 3.3V Power



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