

GM21 LCD TV

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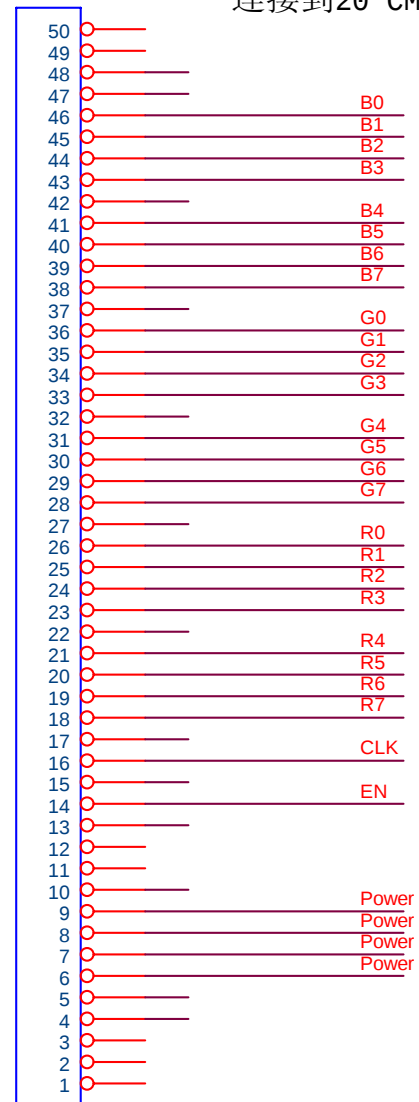
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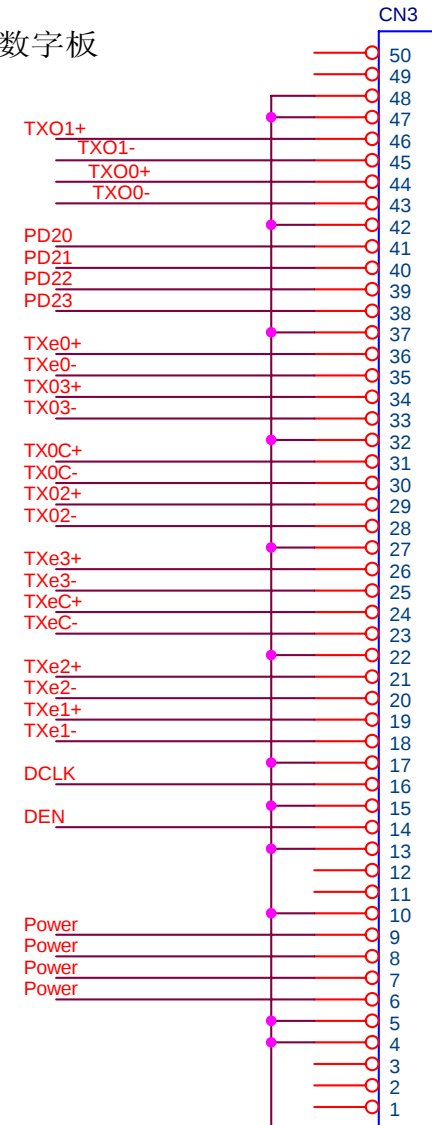
Approval	Organization	Signature	Date
		CHY	04-05-17

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CN3 连接到20"CMO屏

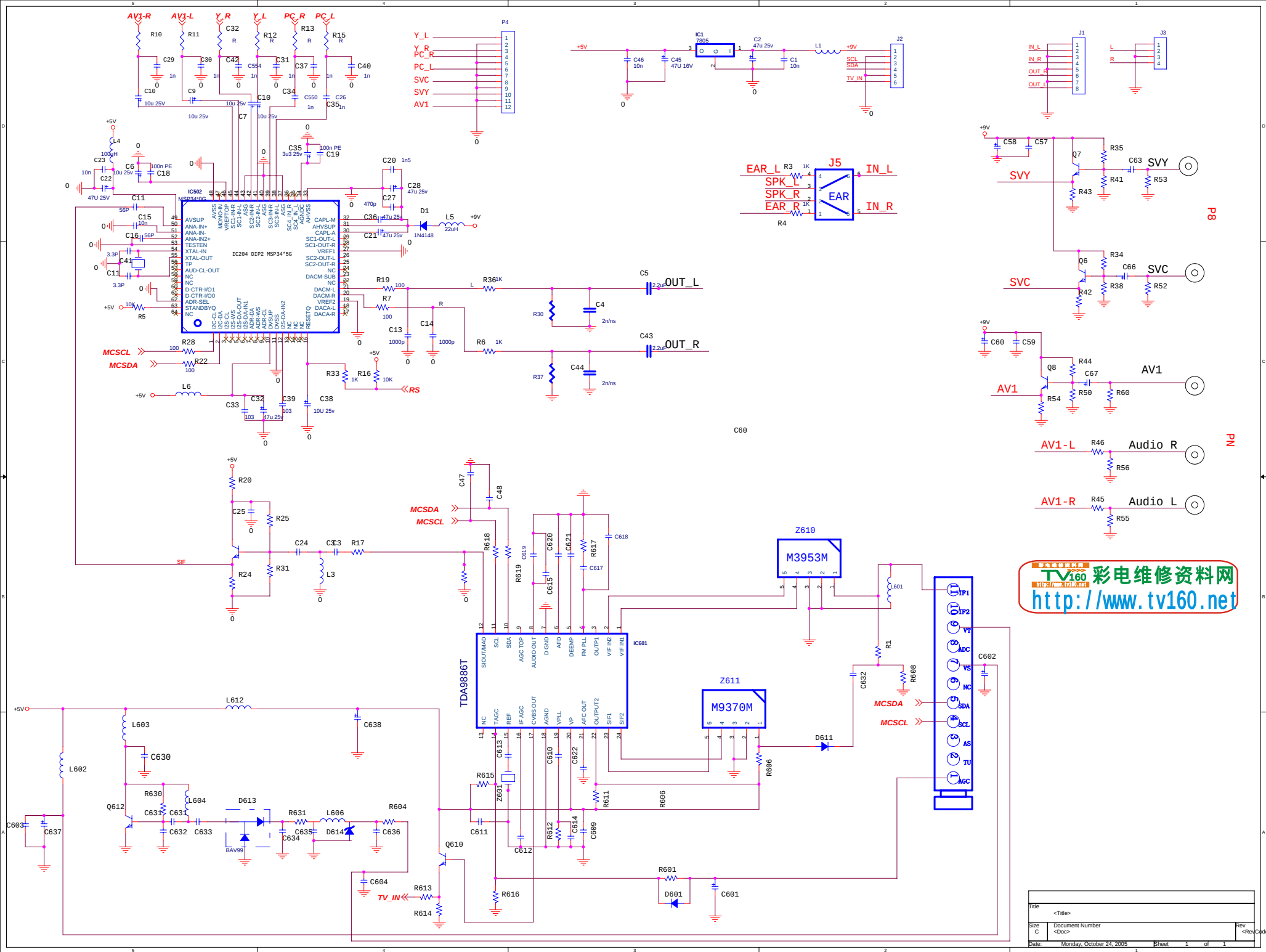


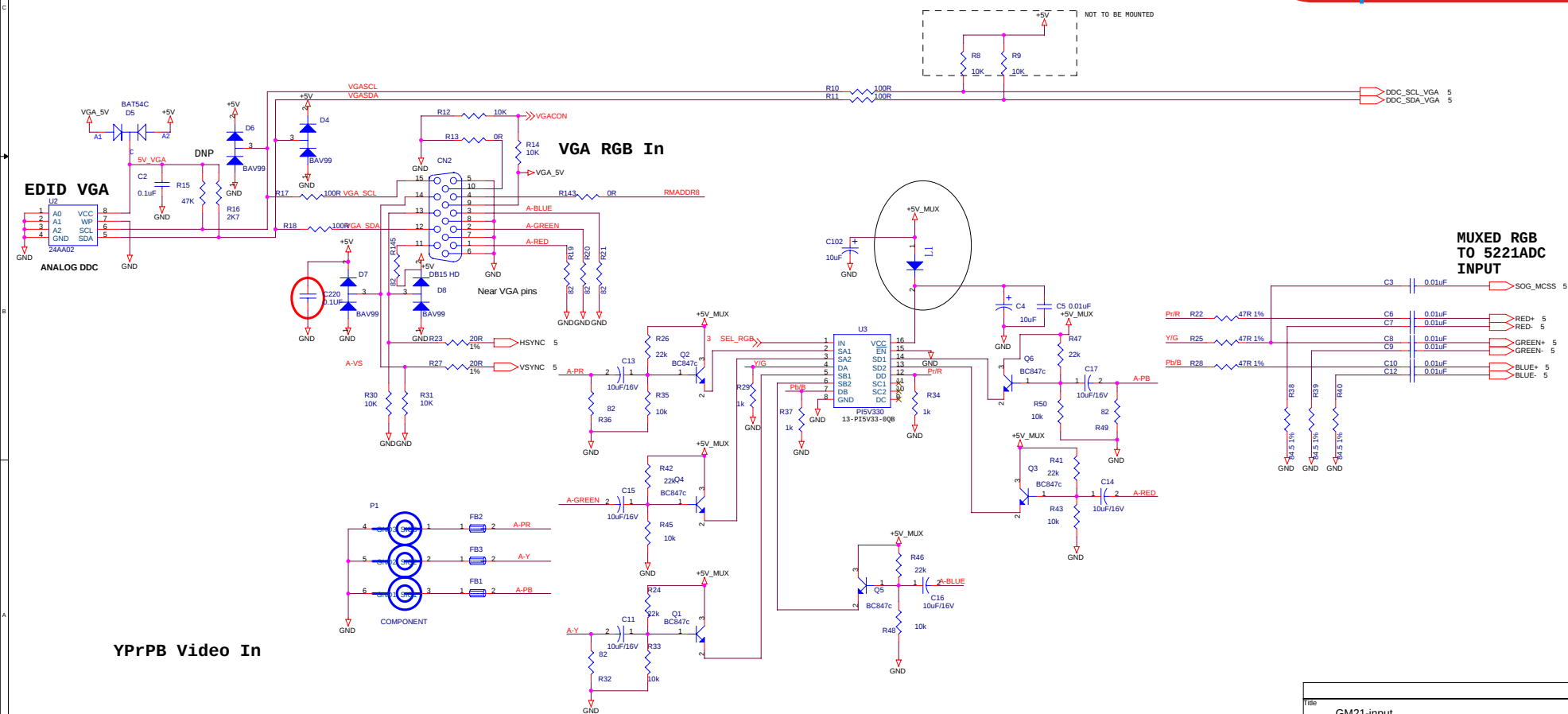
一一对应连接到数字板

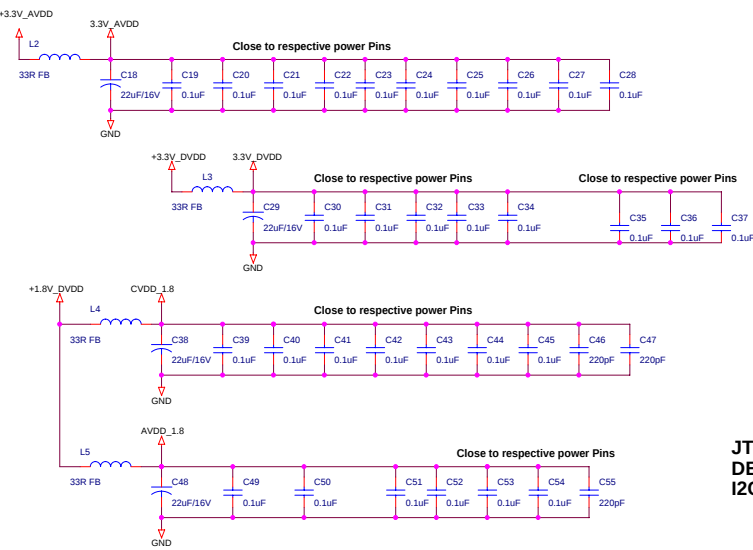


FH12-50S-0.5SH

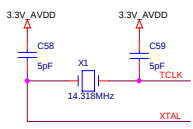
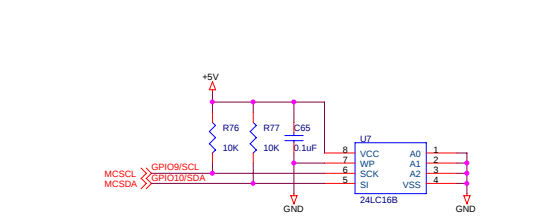
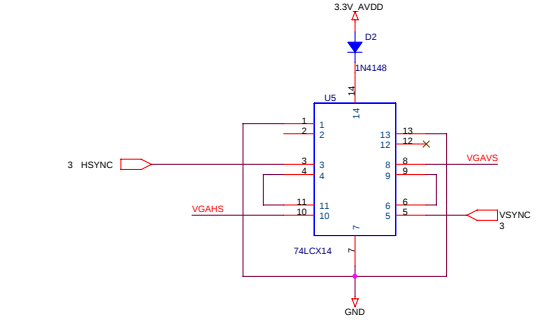
GND





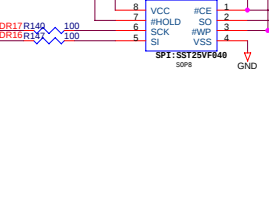
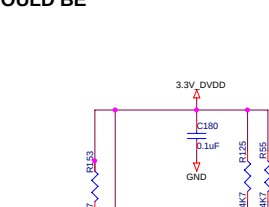
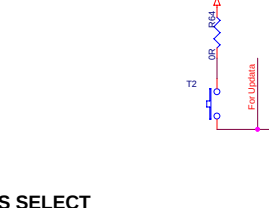
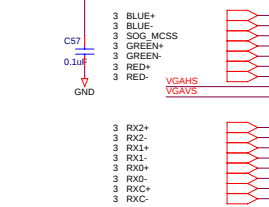
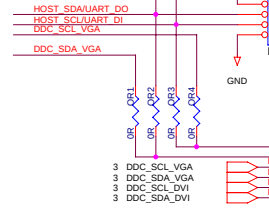


Bootstrap Signals	
RMADDR[8:0]	For I2C address [8:0] to JTAG bridge Host VF, to determine device address.
RMADDR[12:7]	User_Bits[5:0] for configuration setting
RMADDR[14:13]	OP_MODE[1:0]: 00 = Normal op. UART in 186 on system pins. 01 = DC to JTAG bridge. 10 = JTAG port, 5 wires 11 = External parallel control bus using ROM Addr/Data
RMADDR15	SPI_EN: 0 = parallel ROM IF. 1 = SPI serial ROM and Cache control
RMADDR16	Initial state of OCM ROM: 0 = internal ROM on, and mapped to top 32K of OCM and OCM boot will be from internal ROM code 1 = internal ROM off. The external ROM mapped to entire upper 512K of OCM address. OCM boot from external ROM code.
RMADDR17	OSC_SEL: 0 = Xtal and internal oscillator. 1 = TTL oscillator (on TCLK pin)

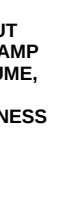
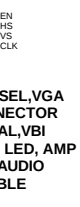
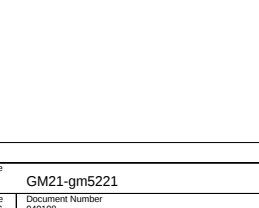
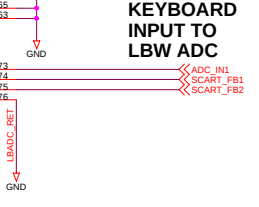
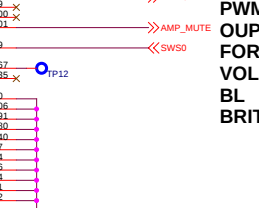
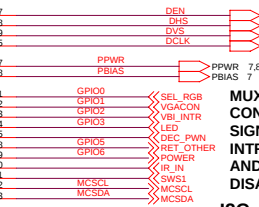
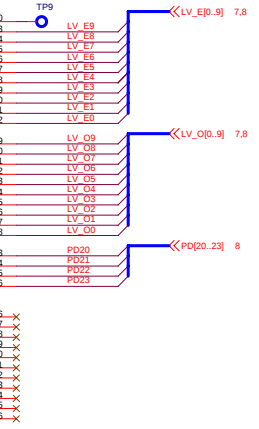
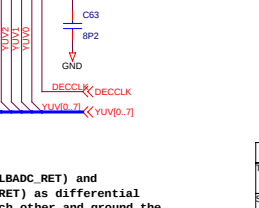
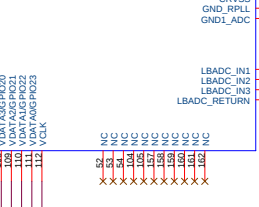
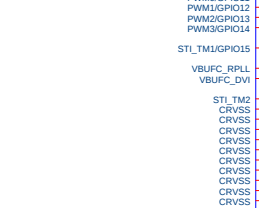
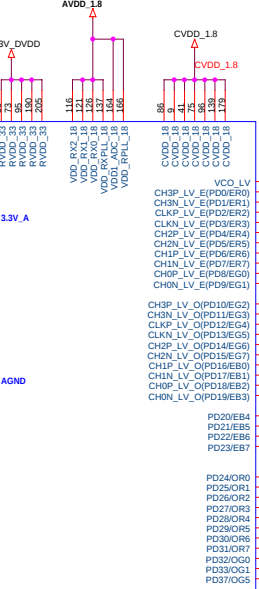
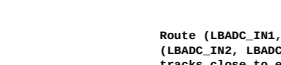
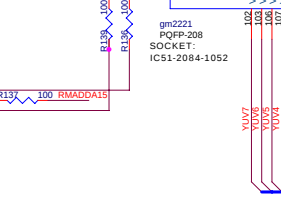
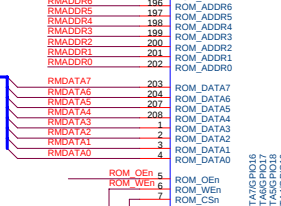
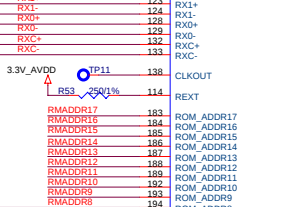
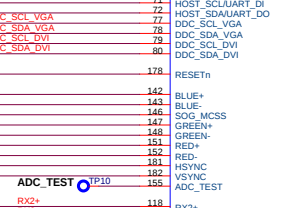
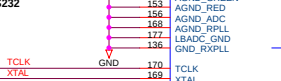


BOOTSTRAP OPTIONS SELECT (NOT POPULATED SHOULD BE HARD WIRED)

**JTAG
DEBUG
I2C SEL**



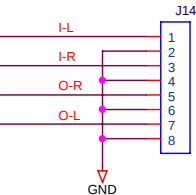
**GPROBE
DEBUG
PORT**



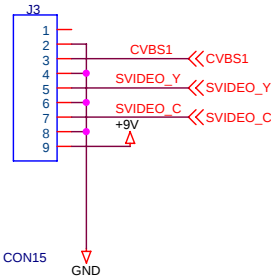
Route (LBADC_IN1, LBADC_RET) and (LBADC_IN2, LBADC_RET) as differential tracks close to each other and ground the return track of each pair very close to the 5221 and ground pin

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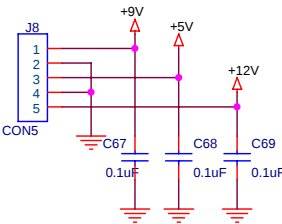
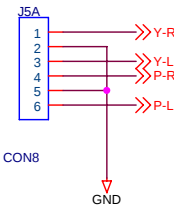
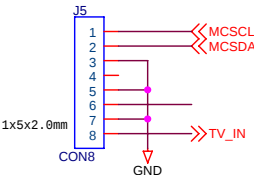
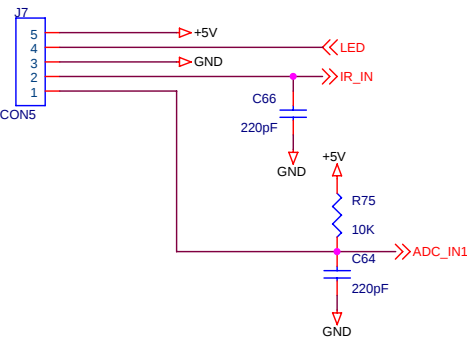
Keypad
INTERFACE



NV RAM
INTERFACE

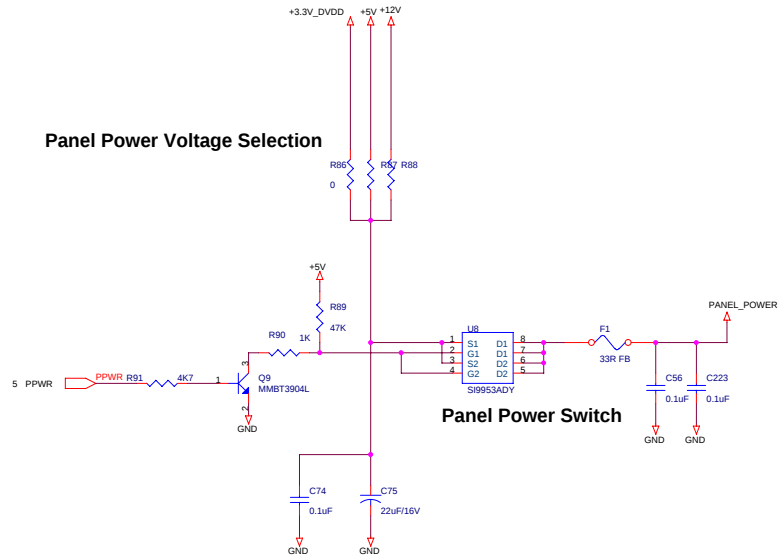


IR REMOTE SENSOR
INTERFACE



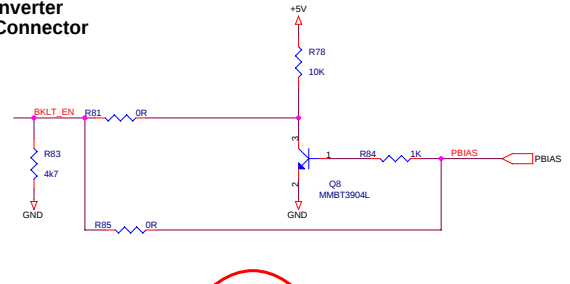
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Panel Power Voltage Selection



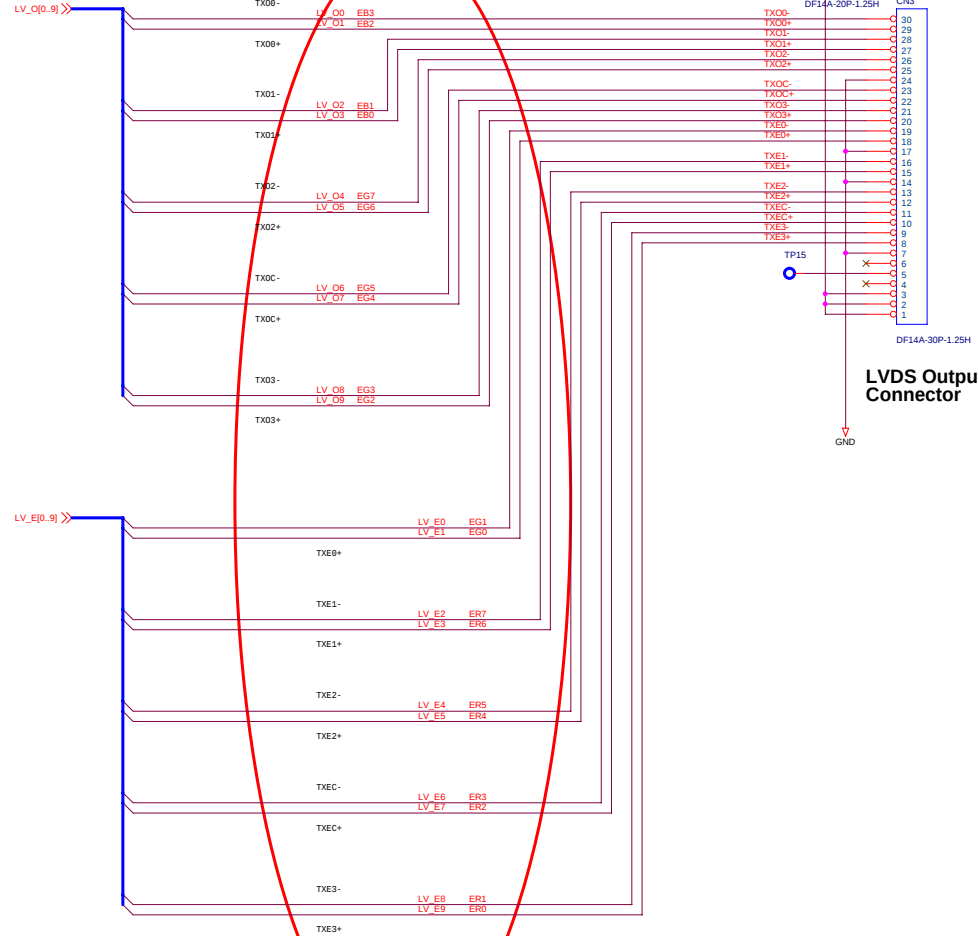
Panel Power Switch

Backlight Inverter Connector

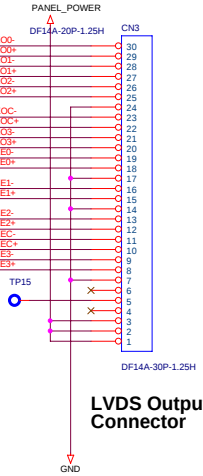


连接到15"SAMSUNG屏

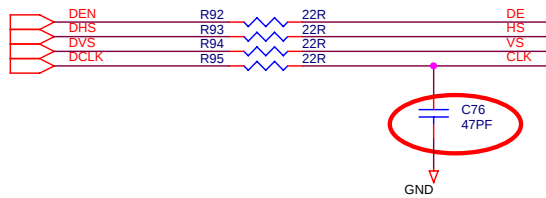
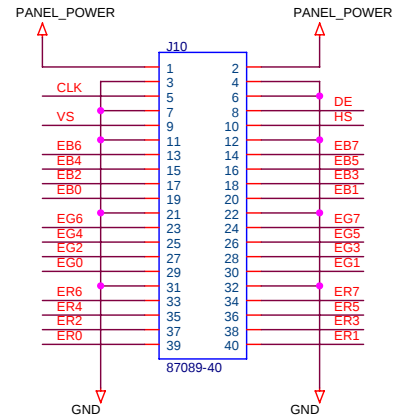
LVDS test points right on the trace to avoid extra length



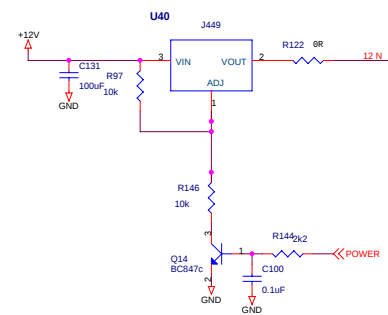
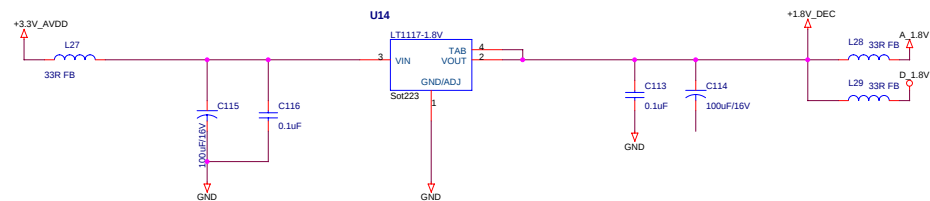
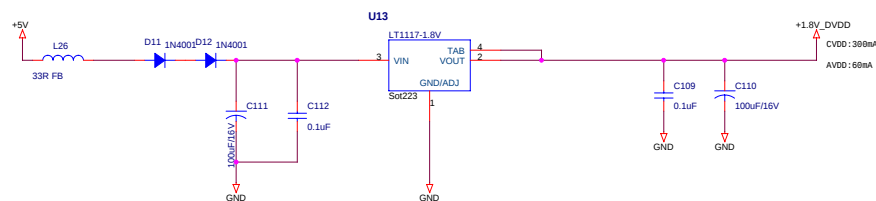
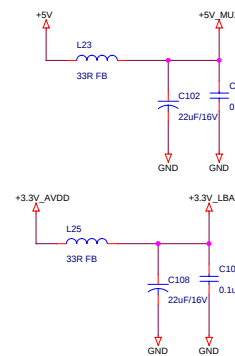
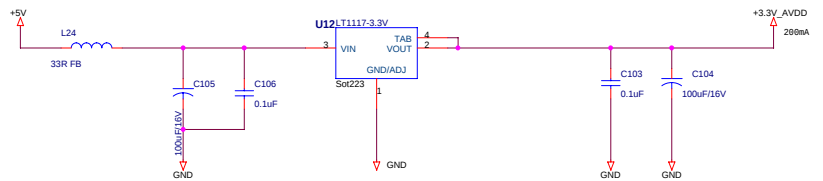
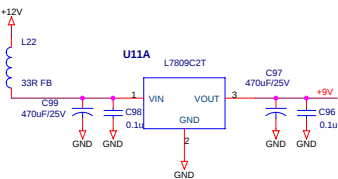
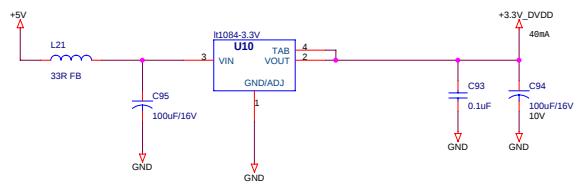
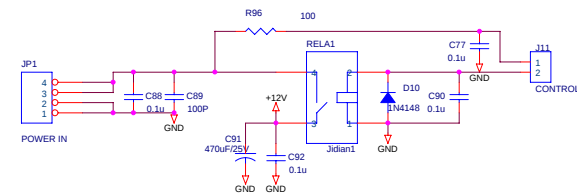
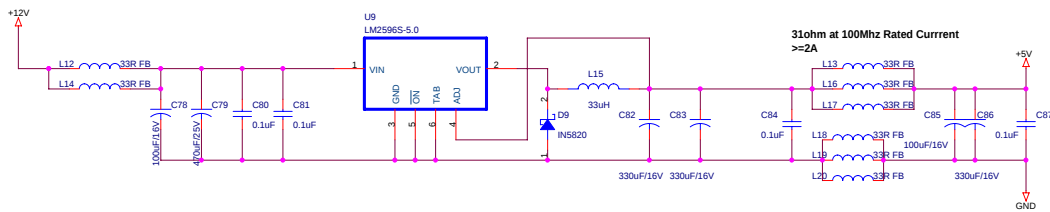
LVDS Output Connector



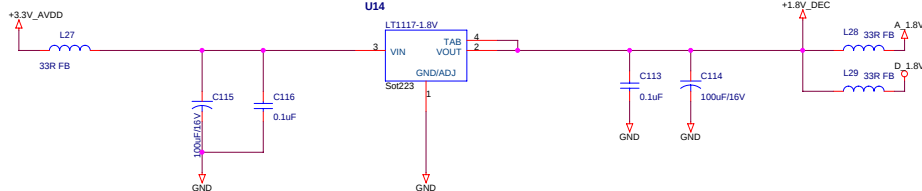
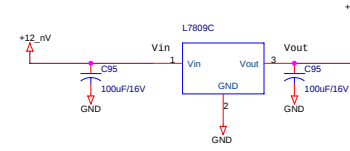
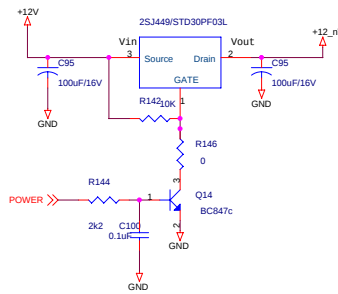
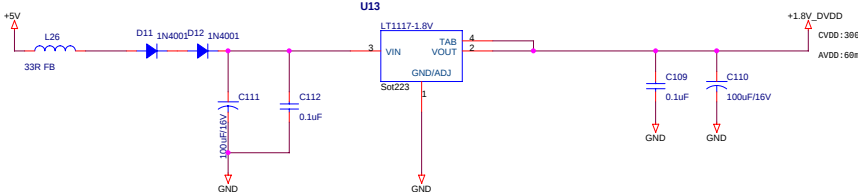
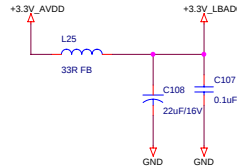
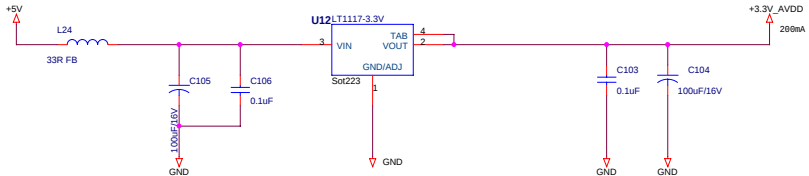
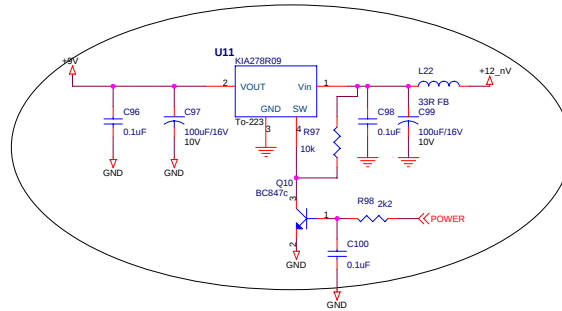
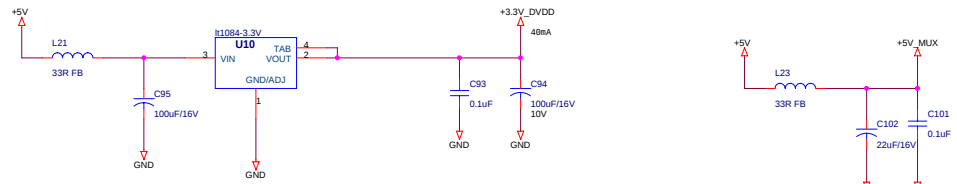
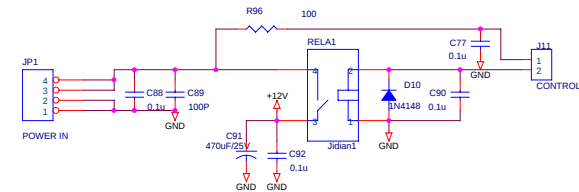
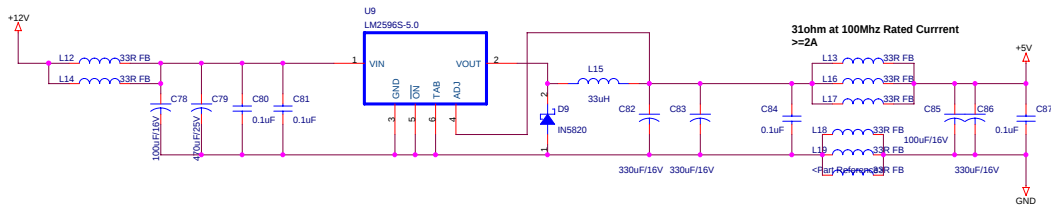
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