power on configration:

AOCLK: H->JTAG; L->GPIO
AMCLK: H->No SDRAM at M2; L->M2 SDRAM Connections
ADATA_1: H->FLASH Connection at M1; L->FLASH Connections at M2
ADATA_0: H->16 bit flash; L-> 8 bit flash

CORE3.3V
R116 10K ADATA0/AL
R117 10K ADATA1/AR
R118 10K AMCLK
R119 NC
R120 10K ASCLK
R121 NC
DGND

M1_A[0:11]
M1_D[0:15]
CORE1.2V
DGND
DGND
CORE3.3V

M1_WE_N M1_CAS_N M1_RAS_N M1_SCS0_N M1_DQM0 M1_DQM1 M1_CLK M1_BA0 M1_BA1 M1_A11 M1_A10 M1_A9 M1_A8 M1_A7 M1_A6 M1_A5 M1_A4 M1_A3 M1_A2 M1_A1 M1_A0 M1_D15 M1_D14 M1_D13 M1_D12 M1_D11 M1_D10 M1_D9 M1_D8 M1_D7 M1_D6 M1_D5 M1_D4 M1_D3 M1_D2 M1_D1 M1_D0

Memory #1

VDD12_1 VDD12_2 VDD12_3 VDD12_4 VDD12_5 VDD12_6 VDD12_7 VSS12_6 VSS12_7 VSS12 VSS12_1 VSS12_2 VSS12_3 VSS12_4 VSS12_5 VSS33 VSS33_1 VSS33_2 VSS33_3 VSS33_4 VSS33_5 VSS33_6 VSS33_7 VSS33_8 VSS33_9 VSS33_10 VSS33_11 VSS33_12 VSS33_13 VSS33_14 VDD33 VDD33_1 VDD33_2 VDD33_3 VDD33_4 VDD33_5 VDD33_6 VDD33_7 VDD33_8 VDD33_9 VDD33_10 VDD33_11 VDD33_12 VDD33_14 VDD33_13

P O W E R

Audio
AMCLK AOCLK ALRCLK ADATA0/AL ADATA1/AR MIO0/ADATA2/U_TX/I2C_M_C MIO1/ADATA3/U_RX/I2C_M_D
AMCLK ASCLK ALRCLK ADATA0/AL ADATA1/AR SI2C_SCL/TX IR/EN/RX
AVDD_DAC

Video DAC
VDD_DAC AVDD_DAC AVDD_R AVDD_G AVDD_B
VSS_DAC AVSS_R AVSS_G AVSS_B
REXT_DAC VREF_DAC COMP
DAC_R DAC_G DAC_B
R/CR/PR G/Y/Y B/CB/PB
at least >=12mil
AVDD_DAC
R114 200R
R115 62R
C107 0.01U
C110 0.1U
C109 100U 16V
C108 0.1U
DGND

ATAPI
AT_D_0 AT_D_1 AT_D_2 AT_D_3 AT_D_4 AT_D_5 AT_D_6 AT_D_7 AT_D_8 AT_D_9 AT_D_10 AT_D_11 AT_D_12 AT_D_13 AT_D_14 AT_D_15
AT_DA2 AT_DA1 AT_DA0 AT_IRQ14 AT_CS0 AT_CS1 AT_DMARQ AT_DMACK_N AT_DIORDY AT_DIOW AT_DIOR
MUTE

U101
AML7218

F_NCS F_NOE
M2_D[0:7] M2_D0 M2_D1 M2_D2 M2_D3 M2_D4 M2_D5 M2_D6 M2_D7
M2_A[0:21] M2_A18 M2_A19 M2_A20 M2_A21
NAND_R/NB NAND_CLE NAND_ALE
M2_A0 M2_A1 M2_A2 M2_A3 M2_A4 M2_A5 M2_A6 M2_A7 M2_A8 M2_A9 M2_A10 M2_A11
M2_WE_N
M2_A15 M2_A14
NAND_CS
M2_A12 M2_A13
M2_A16 M2_A17

FLASH_CS_N FLASH_OE_N M2_D_0/HD_0 M2_D_1/HD_1 M2_D_2/HD_2 M2_D_3/HD_3 M2_D_4/HD_4 M2_D_5/HD_5 M2_D_6/HD_6 M2_D_7HD_7 M2_D_8/HD_15 M2_D_9/HD_14 M2_D_10/HD_13 M2_D_11/HD_12 M2_D_12/HD_11 M2_D_13/HD_10 M2_D_14/HD_9 M2_D_15/HD_8
Memory #2
M2_A_0/PWM2 M2_A_1/PWM3 M2_A_2/HD_HS/PWM0 M2_A_3/HD_VS/PWM1 M2_A_4/T_CPH3 M2_A_5/T_CPV1 M2_A_6/T_CPV2 M2_A_7/T_STV1 M2_A_8/T_STV2 M2_A_9/T_OEV1 M2_A_10/T_OEV2 M2_A_11/T_OEV3
M2_WE_N/HD_16 M2_CAS_N/HD_17 M2_RAS_N/HD_18 M2_SCS0_N/HD_19 M2_SCS1_N/HD_20 M2_DQM0/HD_21 M2_DQM1/HD_22 M2_CLKO/HD_23 M2_BA0/T_STH2 M2_BA1/T_STH1
MIO5/HD_CLK/T_CPH1 AT_CSEL/HD_DE/T_CPH2

SCLK_XIN SCLK_XOUT USB_XIN USB_XOUT DVDD12_PLL3 DVDD12_PLL2 DVDD12_PLL1 AVDD33_PLL3 AVDD33_PLL2 AVDD33_PLL1 DVSS12_PLL3 AVSS33_PLL3 DVSS12_PLL2 AVSS33_PLL2 DVSS12_PLL1 AVSS33_PLL1
CLOCKS & PLL
at least >=12mil
R101 100K
Y101 27M
C101 22P
C102 22P
R102 0R
DVDD AVDD3 AVDD2 AVDD1
DGND

TEST
TMS TDI TCK TDO TEST_N RESET_N
TMS TDI TCK TDO TEST_N RESET_N
C1 100P close to 7218
R103 10K TEST_N
CORE3.3V

NC
NC1 NC2 NC NC3

MIO4/IR MIO3/UART_RX/I2C_D/MIC_IN MIO2/UART_TX/I2C_C
SI2C_SDA PCM1800DATA
C103 100P close to 7218
IIC mode opened

GPIO
EGPIO0/FEC_CLK EGPIO1/FEC_SOP EGPIO2/FEC_VAL EGPIO3/FEC_FAIL EGPIO4/FEC_D0 EGPIO5/FEC_D1 EGPIO12/FEC_D2 EGPIO13/FEC_D3 EGPIO14/FEC_D4 EGPIO15/FEC_D5 EGPIO16/FEC_D6 EGPIO17/FEC_D7

SD/MS
SD/MS_CLK/EGPIO6 SD/MS_CMD/EGPIO7 SD/MS_D0/EGPIO8 SD/MS_D1/EGPIO9 SD/MS_D2/EGPIO10 SD/MS_D3/EGPIO11
EXT_VBO_N1 VBP_1

USB TWO OTG PORTS
ID_USBB VBUS_USBB DP_USBB DM_USBB REXT_USBB VDD12_USB2 VSS12_USB2 VDD33T_USB2 VDD33C_USB2 VSS33T_USB2 VSS33C_USB2 ID_USBA VBUS_USBA DP_USBA DM_USBA REXT_USBA VDD12_USB1 VSS12_USB1 VDD33T_USB1 VDD33C_USB1 VSS33C_USB1 VSS33T_USB1
ID2 VBUS2 DP2 DM2 REXT2
USB1.2V
ID1 VBUS1 DP1 DM1 REXT1
USB3.3V
R110 0R
R111 3K3
R112 3K3
DGND

TS-DEMUX
FEC_CLK/VFD_STB FEC_SOP/VFD_DIN FEC_VALID/VFD_CLK FEC_FAIL/VFD_DO FEC_D7/SPDIF_O FEC_D6/MIC_IN FEC_D5/UART_TX FEC_D4/UART_RX FEC_D3/I2C_S_D FEC_D2/I2C_S_CLK FEC_D1/I2C_M_D FEC_D0/I2C_M_C
I2C_DATA I2C_CLK

CORE3.3V
C106 0.1U
U102 PT7M7809 (VCC GND RESET)
R113 100K
RESET_N
DGND

P101
CORE3.3V
C104 0.1U
R104 4K7
R105 4K7
R106 4K7
R107 4K7
TMS TCK TDO TDI
DGND

U103 M24C02MN
E0/NC E1/NC E2/NC VSS VCC WC SCL SDA
R108 4K7
R109 4K7
I2C_CLK I2C_DATA
C105 0.1U
DGND

U104 PA672T
R130 4K7
R131 4K7
SCL/TX SI2C_SDA/RX
SI2C_SCL/TX
R126 0R IR_IN
R127 0R SDA/RX
R128 4K7
R129 4K7
CORE3.3V
use U104:R129/R131 open,not use U104:open U104/R128/R130
IIC and IR mode open R129/R131

CORE3.3V
R125 4K7
IR/EN
R122 0R SI2C_SDA SI2C_SDA/RX
R123 NC IR/EN/RX
R124 0R IR/EN
I2C MODE: use->R122,R124,R127; open->R123,R126,R129,R130,C103
IR MODE:use->R122,R126,C103; open->R123,R124,R127,R129,R130

CORE1.2V DVDD
FB101 120R
C110 10U 16V
C111 0.1U
C112 0.1U
C113 0.1U
C114 0.1U
DGND

VCC1.2V USB1.2V
FB102 120R
C115 100U 16V
C116 0.1U
C117 0.1U
C118 0.1U
DGND

VCC1.2V CORE1.2V
FB103 120R
C119 100U 16V
C120 0.1U
C121 0.1U
C122 0.1U
C123 0.1U
C124 0.1U
C125 0.1U
C126 0.1U
C127 0.1U
C128 0.1U
DGND

CORE3.3V AVDD1
FB104 120R
C129 47U 16V
C130 0.1U
DGND

CORE3.3V AVDD2
FB105 120R
C131 47U 16V
C132 0.1U
DGND

CORE3.3V AVDD3
FB106 120R
C133 47U 16V
C134 0.1U
DGND

DAC_3.3V AVDD_DAC
FB107 120R
C135 100U 16V
C136 0.1U
C137 0.1U
C138 0.1U
C139 0.1U
C140 0.1U
DGND

DAC_3.3V CORE3.3V
FB108 120R
C141 100U 16V
C142 0.1U
C143 0.1U
C144 0.1U
C145 0.1U
C146 0.1U
C147 0.1U
C148 0.1U
C149 0.1U
C150 0.1U
C151 0.1U
C152 0.1U
C153 0.1U
C154 0.1U
C155 0.1U
C156 0.1U
C157 0.1U
DGND

DAC_3.3V USB3.3V
FB109 120R
C158 100U 16V
C159 0.1U
C160 0.1U
C161 0.1U
C162 0.1U
C163 0.1U
DGND

USE EXTERNAL DAC BE CONNECTED

+5VA
D205 LL4148
R203 330R
D201 LL4148
R201 33K
C202 470U 16V
R202 10K
BT3906 Q201
C201 100U 16V
R204 100K
DGND
Q202 BT3906
R206 1K
MUTE
R205 6K8
CORE3.3V
Q203 BT3904
R207 2K2
R208 4K7

U201
ASCLK
ADATA0/AL
ALRCLK
BCK
DATA
LRCK
DGND
NC
VCC
VOUTL
VOUTR
SCK
FMT
MUTE
DEMP
TEST
ZEROA
VCOM
AGND
AMCLK
PCM1754D
R209 4K7(NC)
C203 47U 16V
C204 0.01U
C205 100U 16V

ADATA0/AL
R210 NC
C206 NC
16V 100U C207
R212 10K
R214 10K
R216 10K
C211 100P
C210 1000P

ADATA1/AR
R211 NC
C208 NC
16V 100U C209
R213 10K
R215 10K
C212 1000P
R217 10K
C213 100P

R222 33K
R223 10K
R224 33K
16V C218 1U
C219 0.1U
C220 0.1U
16V C221 1U

U202
E0/NC
E1/NC
E2/NC
VSS
VCC
WC
SCL
SDA
13-LM833D-00B

C217 100U 16V
R219 330R
ML
R220 1K
Q204 BT3904
C216 2200P
100U C214 16V
R218 330R
MR
R221 1K
Q205 BT3904
C215 2200P

EXTERNAL DAC: open->R210,R211,C206,C208

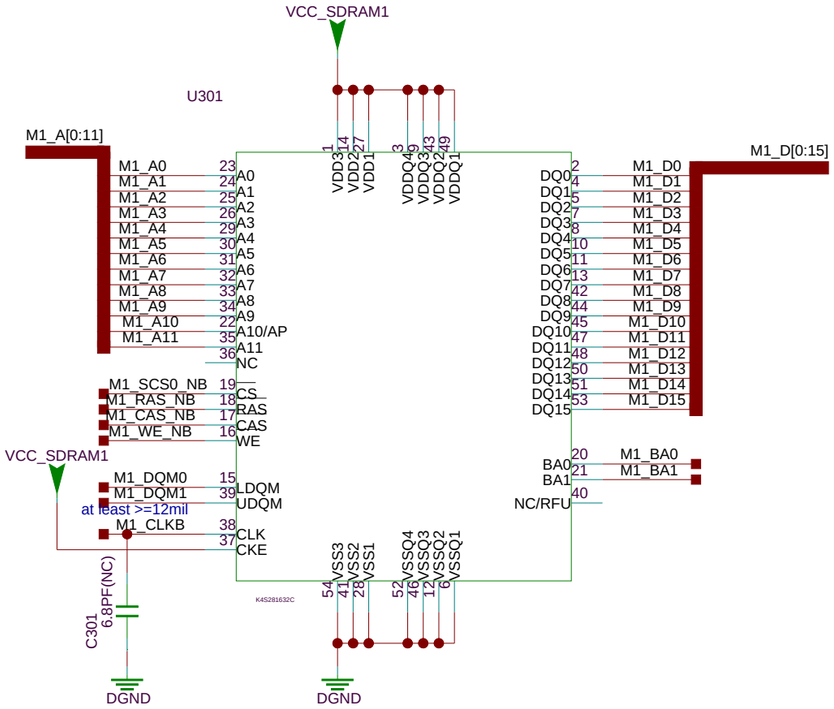
BOM:
If use amplifier of TV, Do not install this block, and R216,R217 value change to 0R.

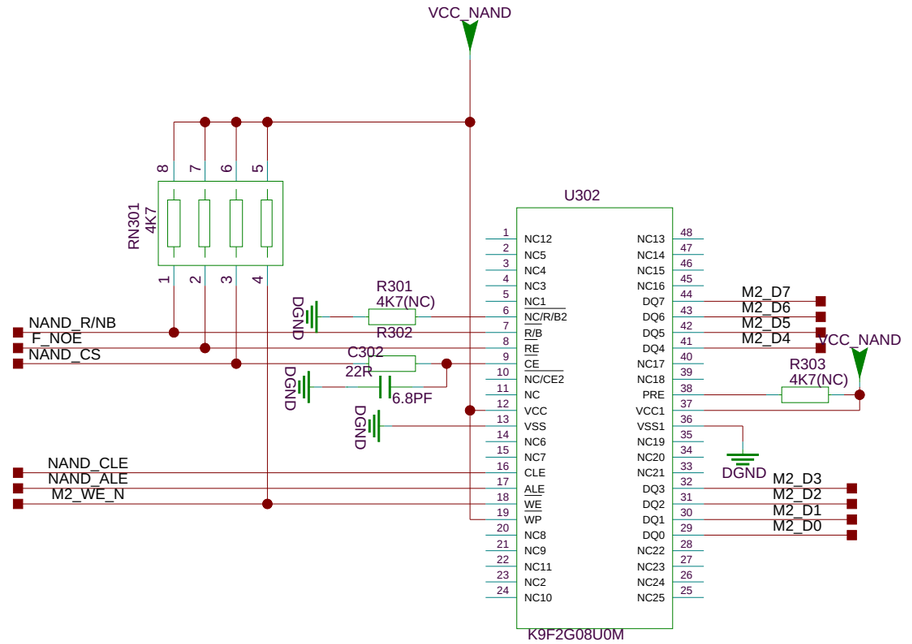
CORE3.3V
0BAV99 D202
G/Y/Y
FB201 0.22UH
Y
R225 75R
C222 22P
C223 100P

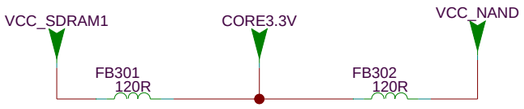
CORE3.3V
0BAV99 D203
B/CB/PB
FB202 0.22UH
PB
R226 75R
C224 22P
C225 100P

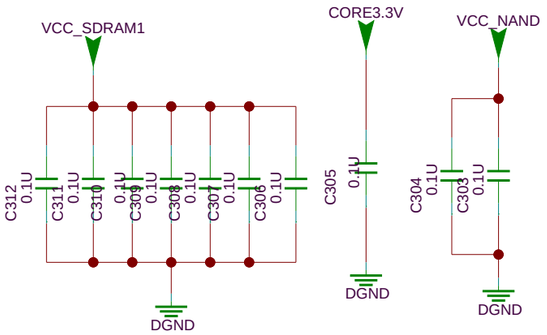
CORE3.3V
0BAV99 D204
R/CR/PR
FB203 0.22UH
PR
R227 75R
C226 22P
C227 100P

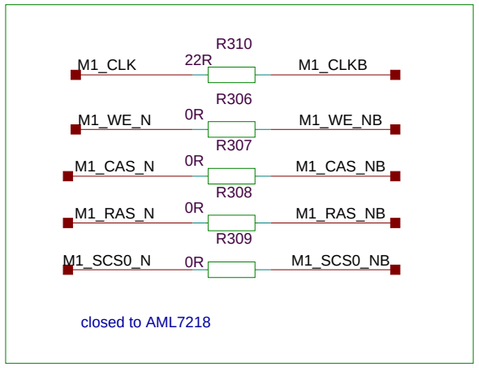
P201
Y
PB
PR
MR
ML

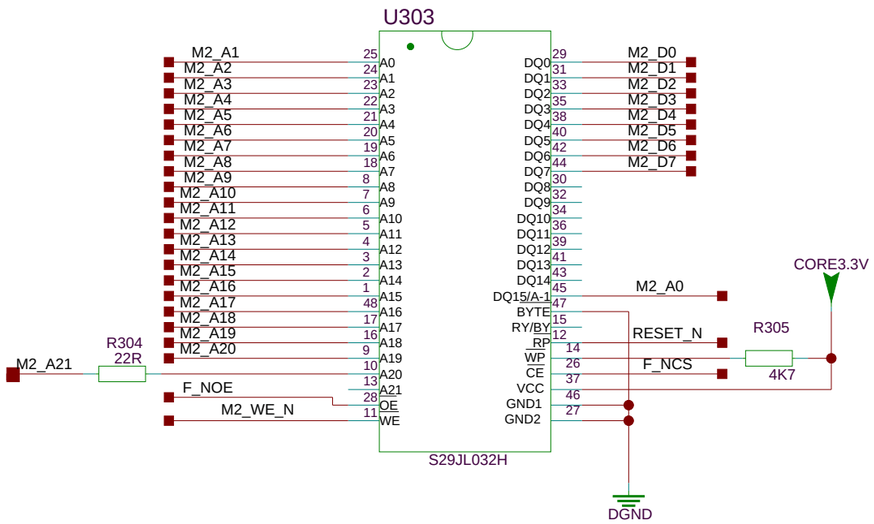

VCC_SDRAM1
U301
M1_A[0:11]
M1_A0
M1_A1
M1_A2
M1_A3
M1_A4
M1_A5
M1_A6
M1_A7
M1_A8
M1_A9
M1_A10
M1_A11
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
NC
M1_SCS0_NB
M1_RAS_NB
M1_CAS_NB
M1_WE_NB
CS
RAS
CAS
WE
M1_DQM0
M1_DQM1
LDQM
UDQM
at least >=12mil
M1_CLKB
CLK
CKE
C301
6.8PF(NC)
DGND
VDD3
VDD2
VDD1
VDDQ4
VDDQ3
VDDQ2
VDDQ1
VSS3
VSS2
VSS1
VSSQ4
VSSQ3
VSSQ2
VSSQ1
K4S281632C
M1_D[0:15]
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
M1_D0
M1_D1
M1_D2
M1_D3
M1_D4
M1_D5
M1_D6
M1_D7
M1_D8
M1_D9
M1_D10
M1_D11
M1_D12
M1_D13
M1_D14
M1_D15
BA0
BA1
NC/RFU
M1_BA0
M1_BA1
BOM: K4S281632I UC60 replace -TC75

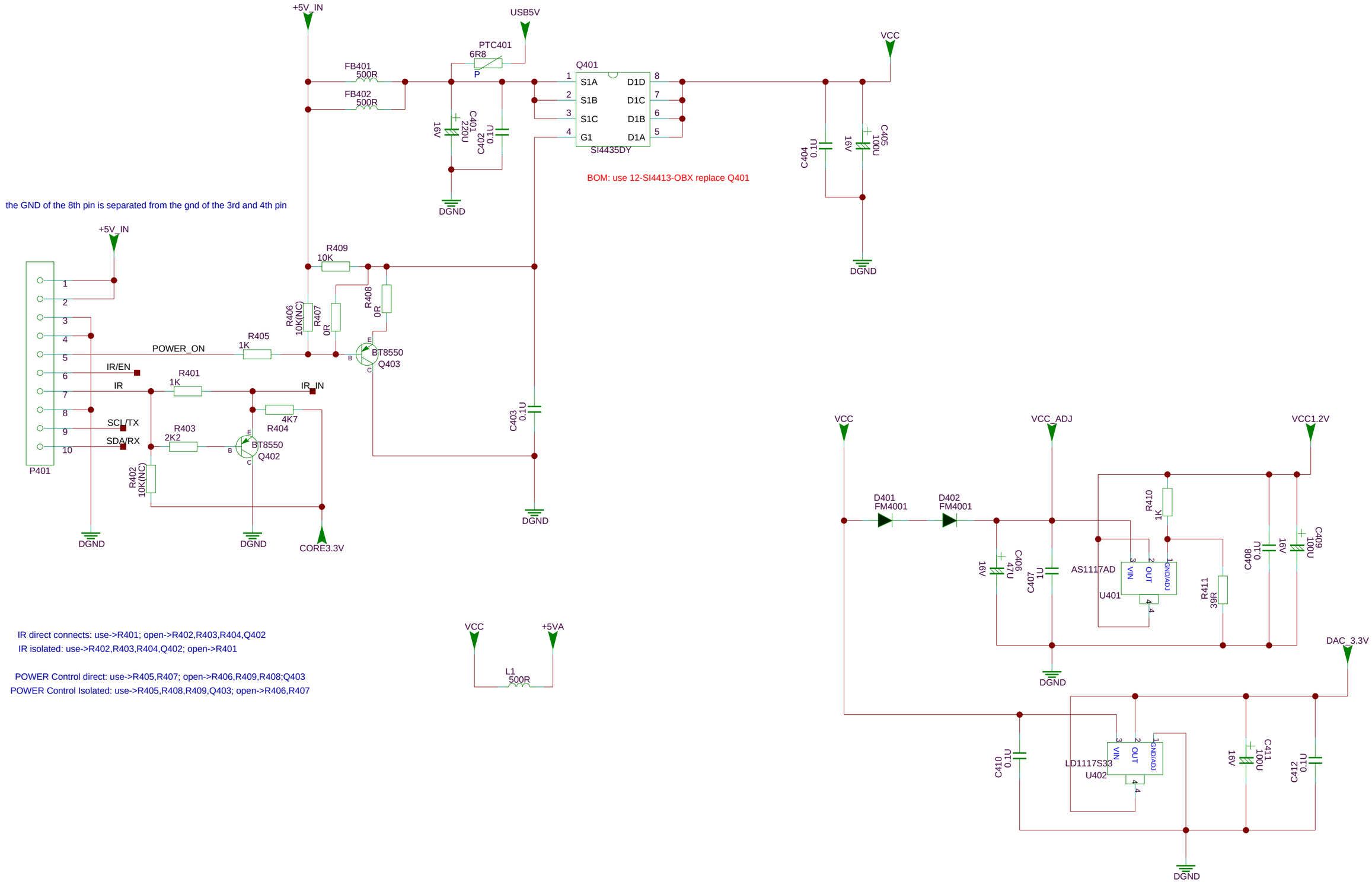

VCC_NAND
RN301
4K7
R301
4K7(NC)
R302
C302
22R
6.8PF
DGND
NAND_R/NB
F_NOE
NAND_CS
NAND_CLE
NAND_ALE
M2_WE_N
U302
NC12
NC5
NC4
NC3
NC1
NC/R/B2
R/B
RE
CE
NC/CE2
NC
VCC
VSS
NC6
NC7
CLE
ALE
WE
WP
NC8
NC9
NC11
NC2
NC10
NC13
NC14
NC15
NC16
DQ7
DQ6
DQ5
DQ4
NC17
NC18
PRE
VCC1
VSS1
NC19
NC20
NC21
DQ3
DQ2
DQ1
DQ0
NC22
NC23
NC24
NC25
M2_D7
M2_D6
M2_D5
M2_D4
M2_D3
M2_D2
M2_D1
M2_D0
R303
4K7(NC)
K9F2G08U0M

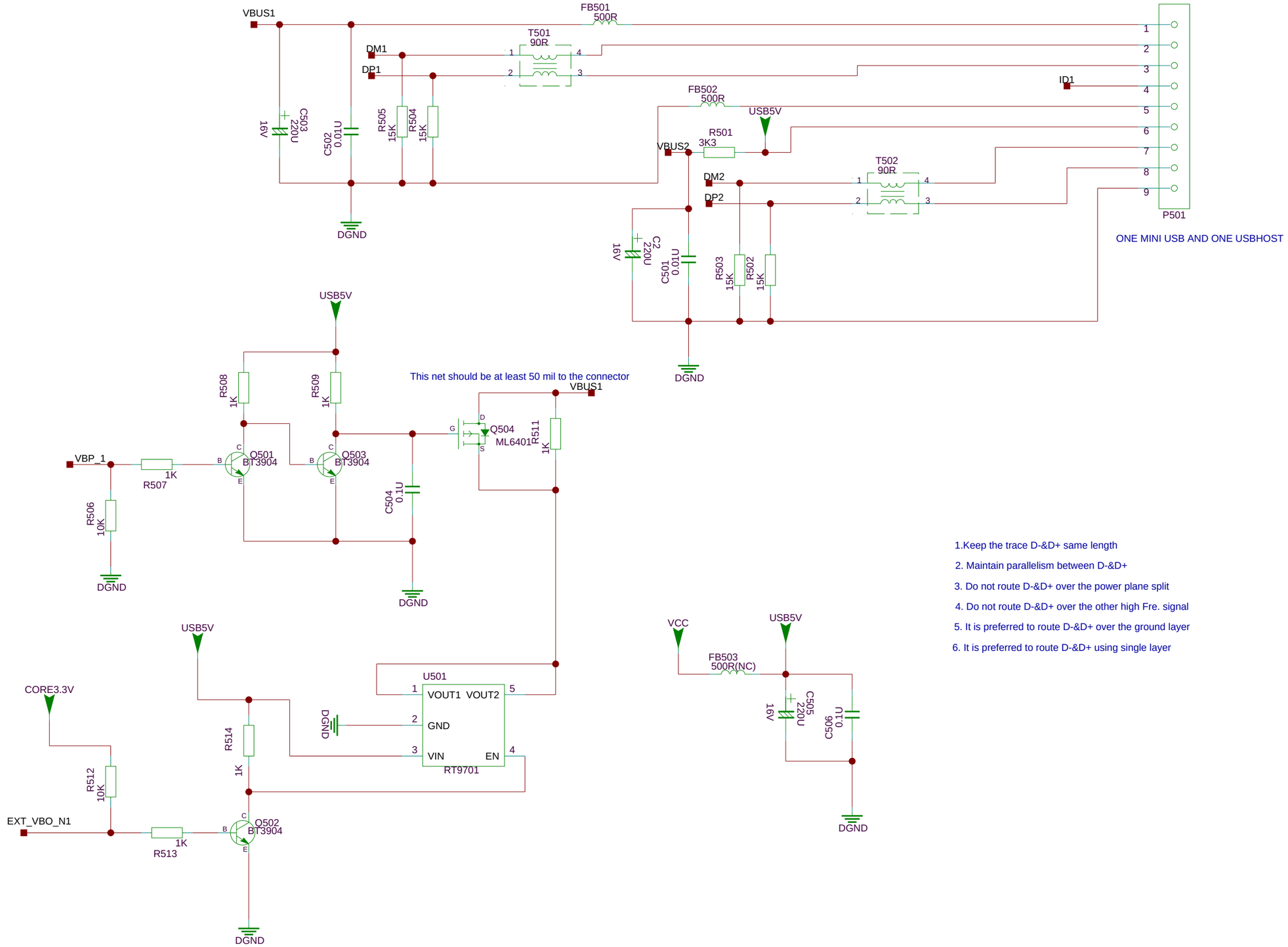

VCC_SDRAM1
CORE3.3V
VCC_NAND
FB301
120R
FB302
120R

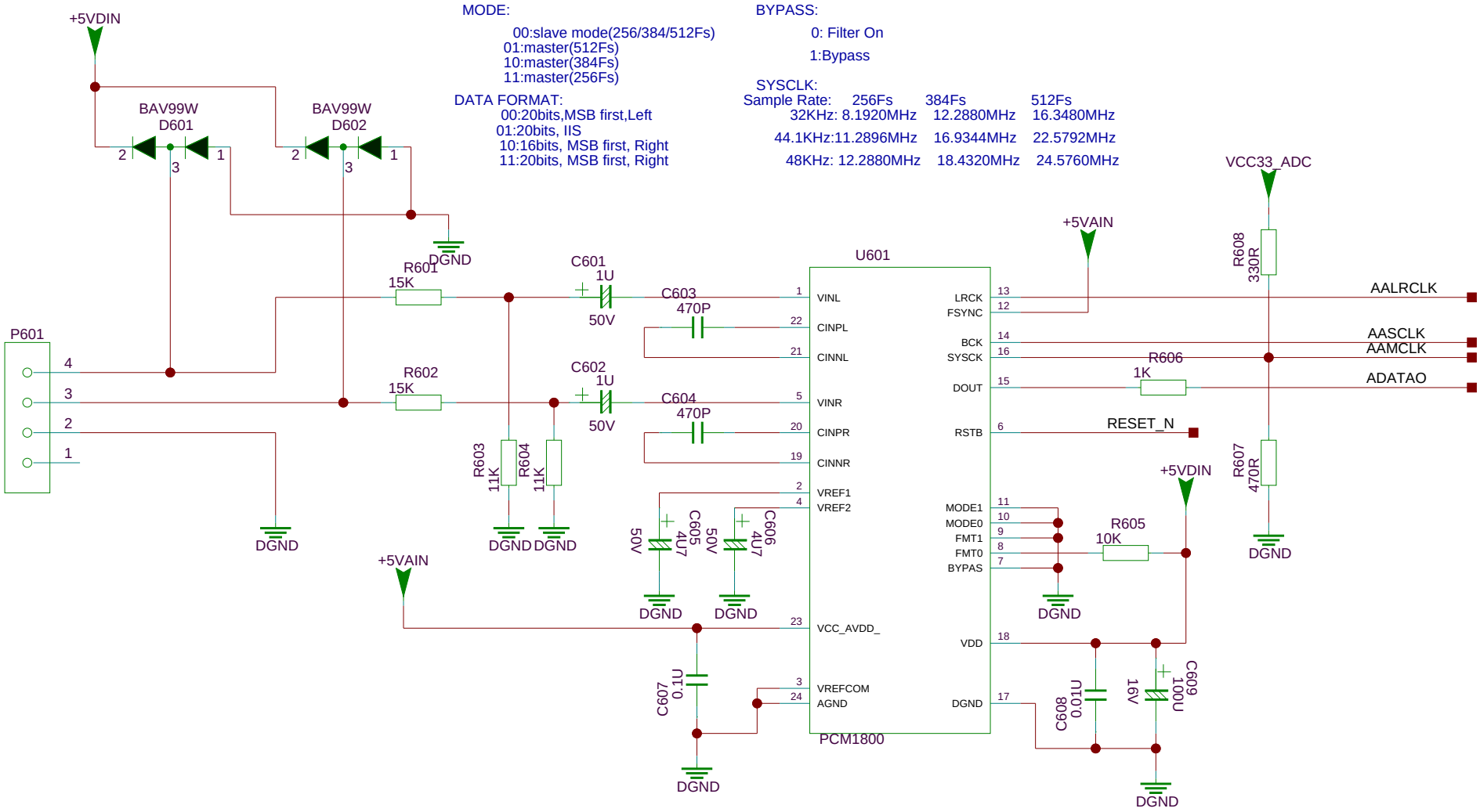

VCC_SDRAM1
C312
C311
C310
C309
C308
C307
C306
0.1U
DGND
CORE3.3V
C305
0.1U
DGND
VCC_NAND
C304
C303
0.1U
DGND


R310
M1_CLK
22R
M1_CLKB
R306
M1_WE_N
0R
M1_WE_NB
R307
M1_CAS_N
0R
M1_CAS_NB
R308
M1_RAS_N
0R
M1_RAS_NB
R309
M1_SCS0_N
0R
M1_SCS0_NB
closed to AML7218


U303
M2_A1
M2_A2
M2_A3
M2_A4
M2_A5
M2_A6
M2_A7
M2_A8
M2_A9
M2_A10
M2_A11
M2_A12
M2_A13
M2_A14
M2_A15
M2_A16
M2_A17
M2_A18
M2_A19
M2_A20
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
OE
WE
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15/A-1
BYTE
RY/BY
RP
WP
CE
VCC
GND1
GND2
M2_D0
M2_D1
M2_D2
M2_D3
M2_D4
M2_D5
M2_D6
M2_D7
M2_A0
RESET_N
F_NCS
R304
22R
M2_A21
F_NOE
M2_WE_N
R305
4K7
CORE3.3V
DGND
S29JL032H


+5V_IN
USB5V
PTC401
6R8
P
FB401
500R
FB402
500R
Q401
S1A
S1B
S1C
G1
D1D
D1C
D1B
D1A
SI4435DY
C401
220U
16V
C402
0.1U
DGND
VCC
C404
0.1U
C405
100U
16V
DGND
BOM: use 12-SI4413-OBX replace Q401
the GND of the 8th pin is separated from the gnd of the 3rd and 4th pin
+5V_IN
R409
10K
R406
10K(NC)
R407
0R
R408
0R
R405
1K
POWER_ON
BT8550
Q403
IR/EN
R401
1K
IR
IR_IN
4K7
R404
SCL/TX
SDA/RX
R403
2K2
BT8550
Q402
R402
10K(NC)
P401
DGND
DGND
CORE3.3V
C403
0.1U
DGND
VCC
+5VA
L1
500R
VCC
VCC_ADJ
VCC1.2V
D401
FM4001
D402
FM4001
R410
1K
C406
47U
16V
C407
1U
AS1117AD
U401
VIN
OUT
GND/ADJ
R411
39R
C408
0.1U
16V
C409
100U
DGND
DAC_3.3V
C410
0.1U
LD1117S33
U402
VIN
OUT
GND/ADJ
C411
100U
16V
C412
0.1U
DGND
IR direct connects: use->R401; open->R402,R403,R404,Q402
IR isolated: use->R402,R403,R404,Q402; open->R401
POWER Control direct: use->R405,R407; open->R406,R409,R408;Q403
POWER Control Isolated: use->R405,R408,R409,Q403; open->R406,R407


VBUS1
FB501
500R
T501
90R
DM1
DP1
1
2
3
4
ID1
FB502
500R
USB5V
R501
3K3
VBUS2
T502
90R
DM2
DP2
C503
220U
16V
C502
0.01U
R505
15K
R504
15K
DGND
C2
220U
16V
C501
0.01U
R503
15K
R502
15K
P501
5
6
7
8
9
ONE MINI USB AND ONE USBHOST
USB5V
R508
1K
R509
1K
This net should be at least 50 mil to the connector
VBUS1
D
G
S
Q504
ML6401
R511
1K
VBP_1
C
B
E
Q501
BT3904
Q503
BT3904
1K
R507
R506
10K
C504
0.1U
DGND
DGND
USB5V
U501
VOUT1
VOUT2
GND
VIN
EN
RT9701
CORE3.3V
R514
1K
R512
10K
EXT_VBO_N1
Q502
BT3904
1K
R513
DGND
VCC
USB5V
FB503
500R(NC)
C505
220U
16V
C506
0.1U
DGND
1.Keep the trace D-&D+ same length
2. Maintain parallelism between D-&D+
3. Do not route D-&D+ over the power plane split
4. Do not route D-&D+ over the other high Fre. signal
5. It is preferred to route D-&D+ over the ground layer
6. It is preferred to route D-&D+ using single layer


MODE:
00:slave mode(256/384/512Fs)
01:master(512Fs)
10:master(384Fs)
11:master(256Fs)
DATA FORMAT:
00:20bits,MSB first,Left
01:20bits, IIS
10:16bits, MSB first, Right
11:20bits, MSB first, Right
BYPASS:
0: Filter On
1:Bypass
SYSCLK:
Sample Rate: 256Fs 384Fs 512Fs
32KHz: 8.1920MHz 12.2880MHz 16.3480MHz
44.1KHz:11.2896MHz 16.9344MHz 22.5792MHz
48KHz: 12.2880MHz 18.4320MHz 24.5760MHz
+5VDIN
BAV99W
D601
D602
DGND
R601
15K
R602
15K
C601
1U
50V
C602
1U
50V
C603
470P
C604
470P
P601
R603
11K
R604
11K
C605
4U7
50V
C606
4U7
50V
U601
VINL
CINPL
CINNL
VINR
CINPR
CINNR
VREF1
VREF2
VCC_AVDD_
VREFCOM
AGND
PCM1800
LRCK
FSYNC
BCK
SYSCK
DOUT
RSTB
MODE1
MODE0
FMT1
FMT0
BYPAS
VDD
DGND
+5VAIN
VCC33_ADC
R608
330R
R606
1K
R607
470R
R605
10K
C607
0.1U
C608
0.01U
C609
100U
16V
AALRCLK
AASCLK
AAMCLK
ADATAO
RESET_N
Ver C changed: Pin 8 connect to VCC, Pin 9 connect to GND, Pin18 connect to VCC
AMCLK
ASCLK
ALRCLK
ADATAO
R609
22R
R610
22R
R611
22R
R612
0R
AAMCLK
AASCLK
AALRCLK
PCM1800DATA
+5VA
FB601
500R
FB602
500R
C610
0.1U
C611
100U
16V
C612
0.1U
FB603
500R
C613
0.1U
DAC_3.3V